UNIT-V

ARCHITECTURE OF TMS320c50

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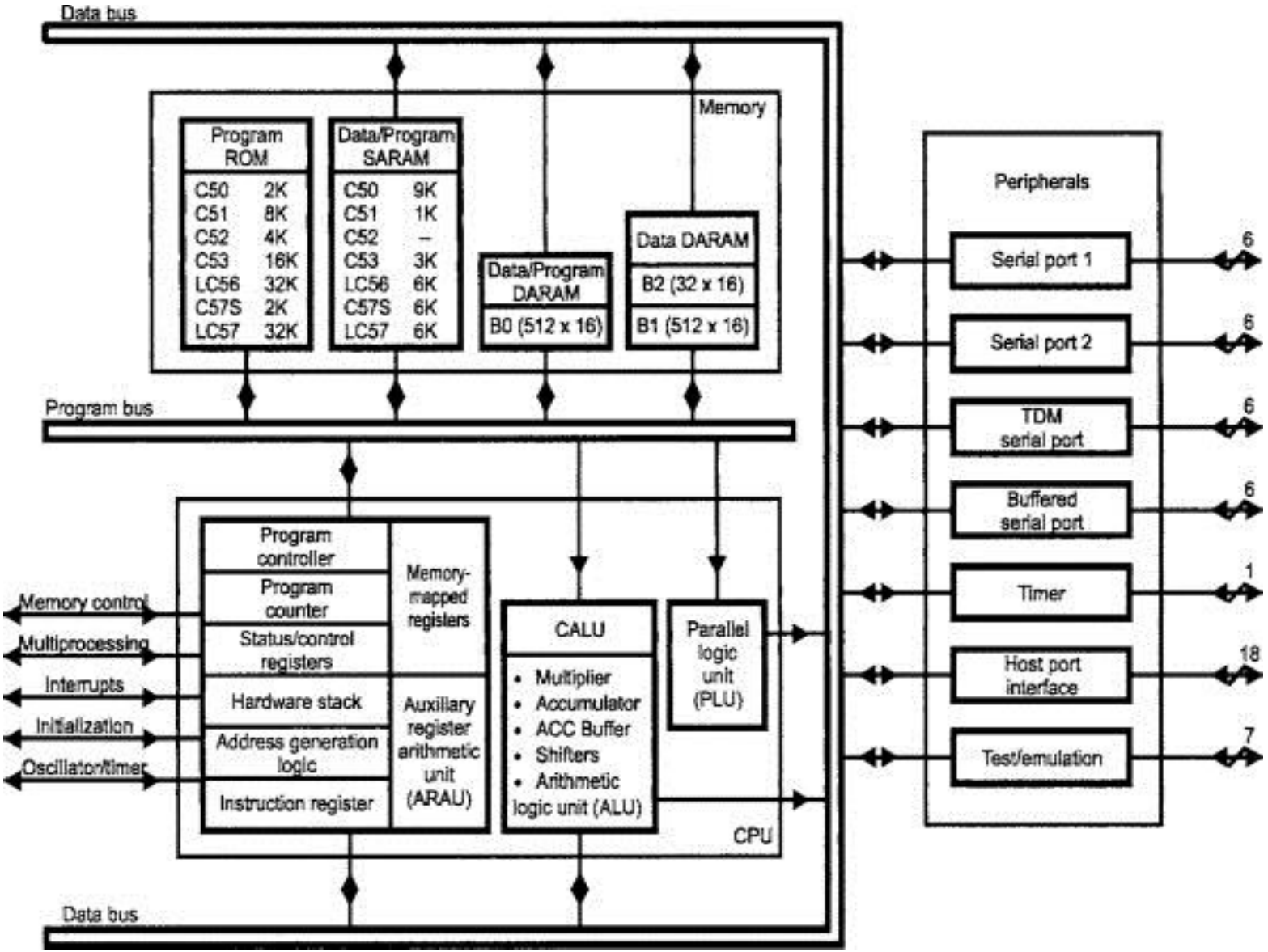
Features

- Fabricated with CMOS IC Technology.
- Fixed point, 16 bit processor running at 40MHz.
- Single instruction execution time is 50nsec.
- Architectural design based on combination of advanced Harvard architecture, onchip peripherals and onchip memory.
- It has highly specialized instruction set.
- These features enable operation flexibility and the device speed.

BLOCK DIAGRAM



Bus structure

i. PB
ii. PAB
iii. DB
iv. DAB

CPU

i. CALU
ii. PLU
iii. ARAU
iv. Memory mapped registers
v. Program controller

Block repeat registers

i. RPTC
ii. BRCR
iii. PASR
iv. PAER

Program Controller

i. Program Counter
ii. Status and Control register
iii. Hardware stack
iv. Address generation logic
v. Instruction register

On-chip memory

Total memory address range of 224k x 16bits

The memory space is divided into four memory segments

64k word Program memory space

64k word local data memory space

64k word input / output ports

32k word Global data memory space

i. Program read only memory
ii. Data/Program single access RAM (SARAM)
iii. Data/Program dual access RAM (DARAM)

On-chip Peripherals

i. Clock generator
ii. Hardware timer
iii. Software programmable wait state generators
iv. General purpose I/O ports
v. Parallel I/O ports
vi. Serial port interface
vii. Buffered serial port
viii. Time division multiplexed (TDM) serial port
ix. Host port interface
x. User unmaskable interrupts

ARCHITECTURE OF TMS320c54x

Features

- It is a 16bit fixed point digital signal processor
- Introduced in Japan in 1994
- Fabricated with an advanced modified Harvard architecture that has

One program memory bus

Three data memory buses

Four address buses

- It runs at 160MHz with 1.6 volt core supply volt

BLOCK DIAGRAM

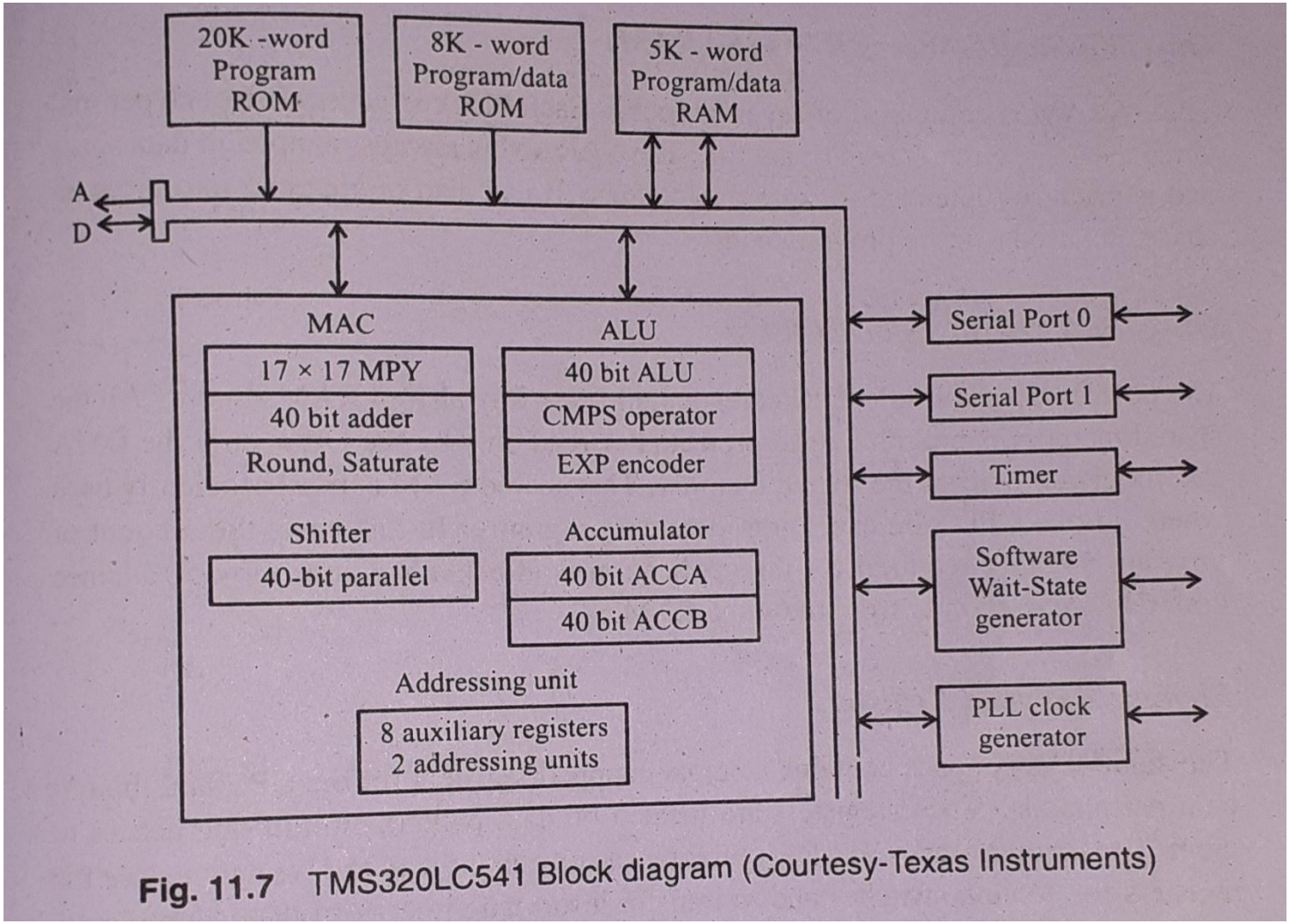


Fig. 11.7 TMS320LC541 Block diagram (Courtesy-Texas Instruments)

- Internal memory organization
- On-chip ROM
- On-chip DARAM
- On-chip SARAM
- On-chip DARAM
- On-chip two way shared RAM
- Memory mapped registers
- CPU
- ALU

Overflow handling

If **OVM=0** the accumulators are loaded with the ALU result without modification

If **OVM=1** the accumulators are loaded with either the most positive 32bit value (00 7FFF FFFFh) or the most negative 32bit value (FF 8000 0000h) depending on the direction of the overflow.

Carry bit

Dual 16 bit mode

Accumulators

ALU

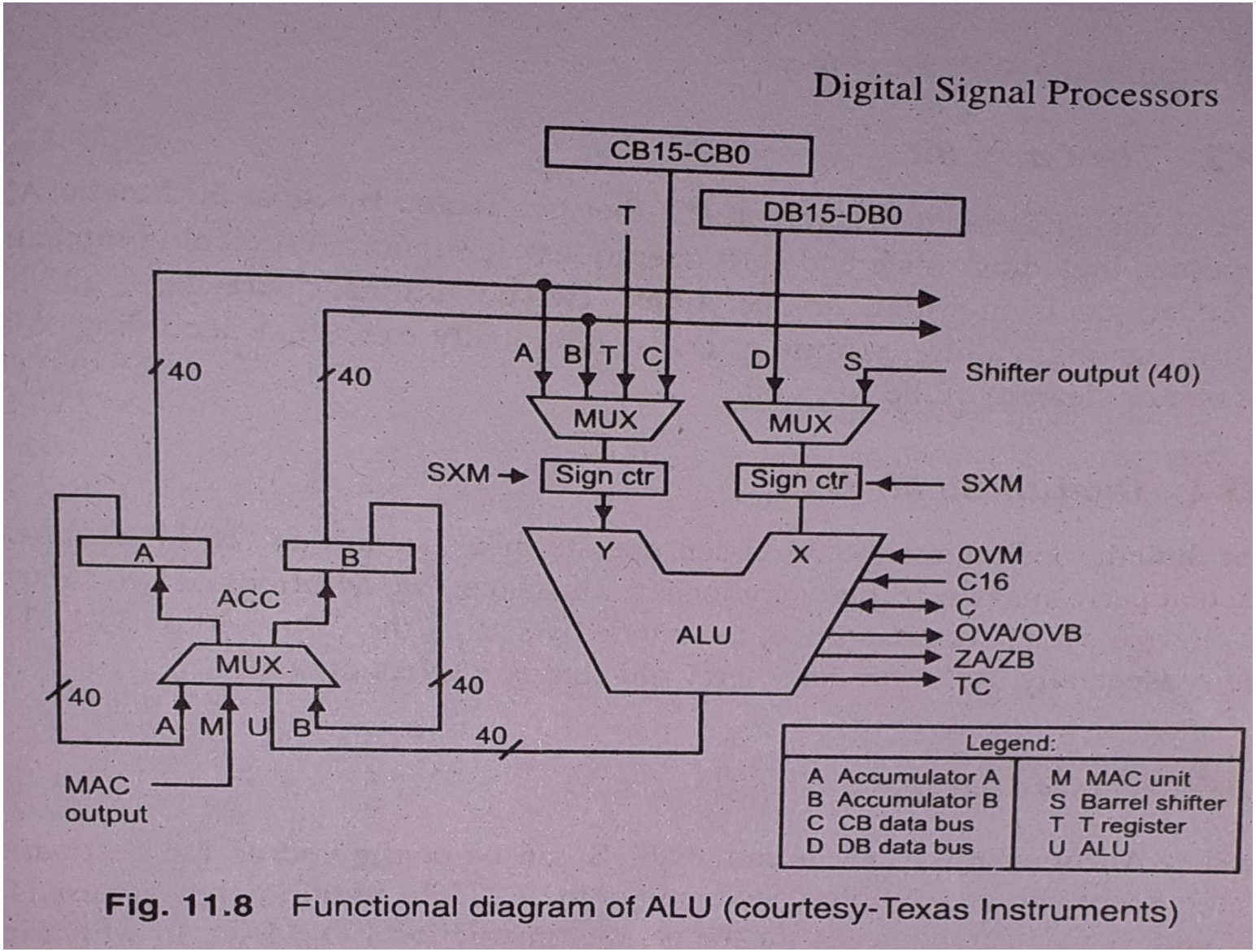


Fig. 11.8 Functional diagram of ALU (courtesy-Texas Instruments)

Barrel shifter

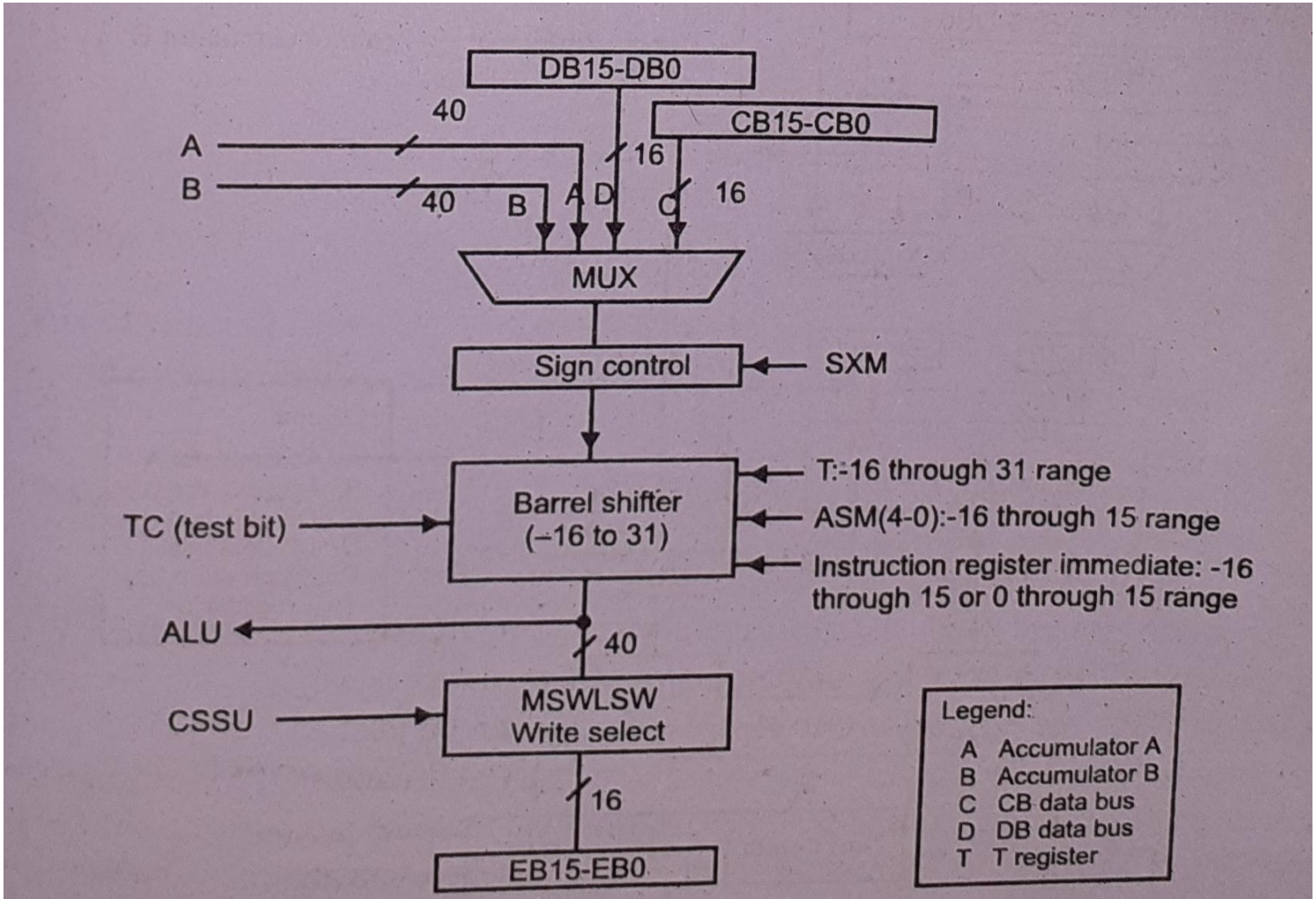


Fig. 11.11 Functional diagram of Barrel shifter (courtesy-Texas Instruments)

Multiplier / Adder Unit

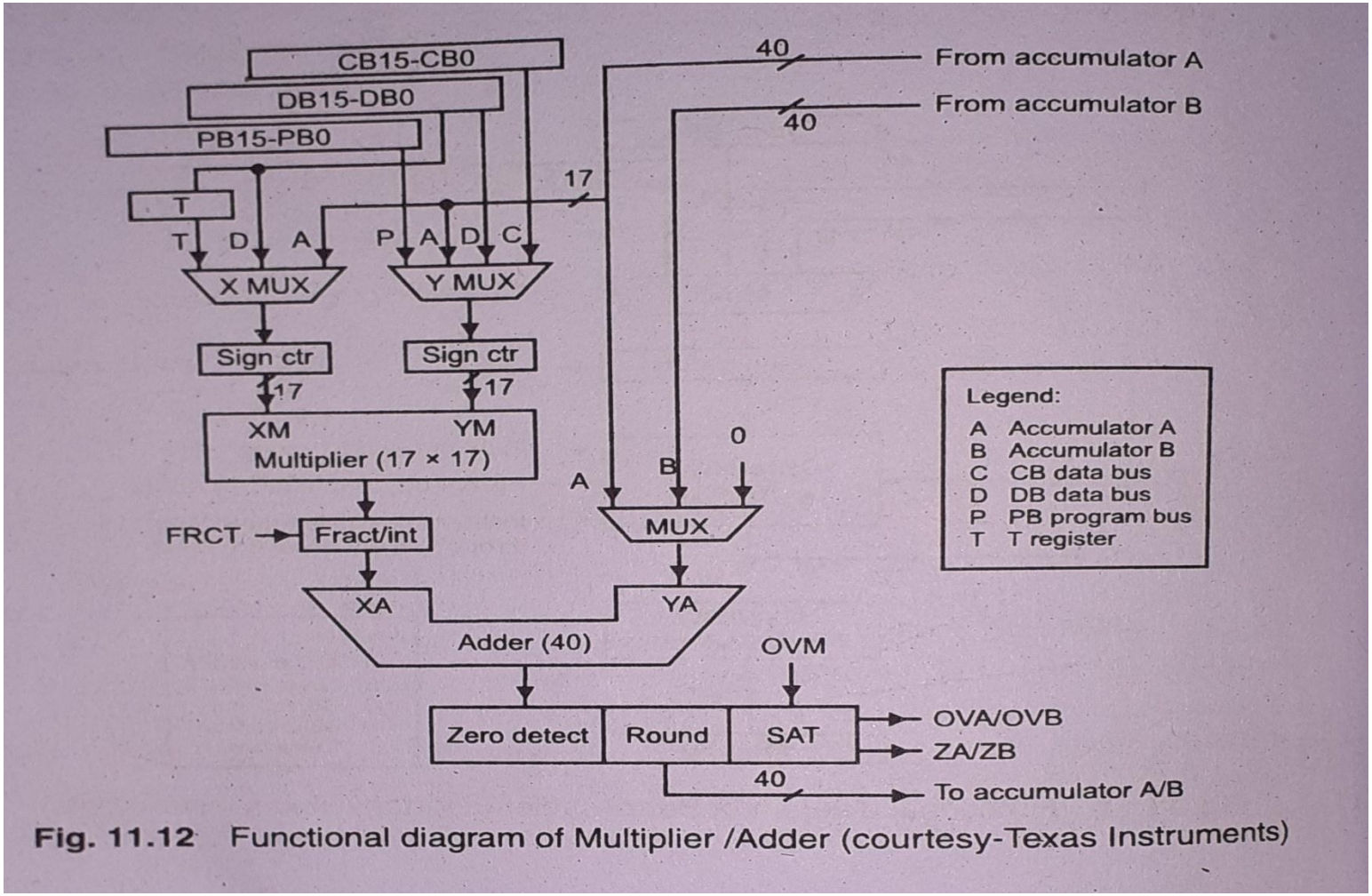


Fig. 11.12 Functional diagram of Multiplier /Adder (courtesy-Texas Instruments)

Compare, Select, Store Unit (CSSU)

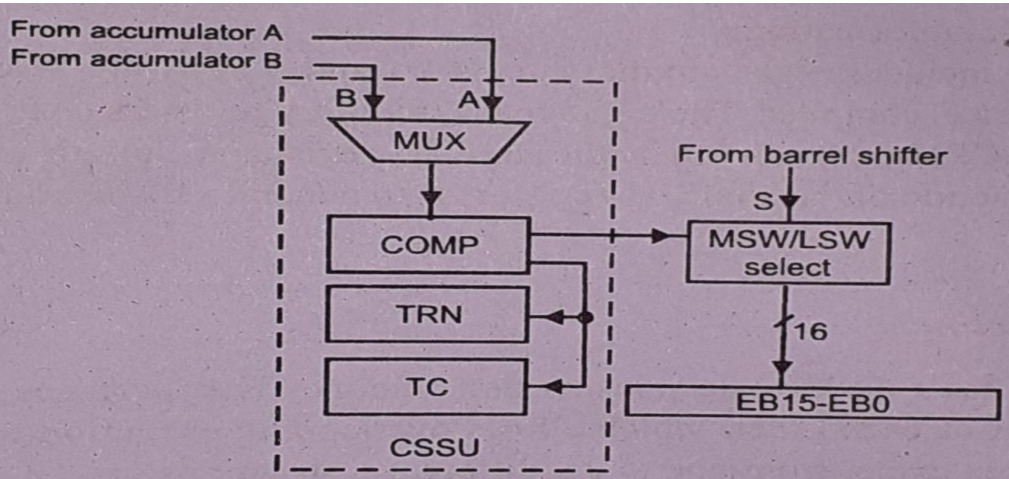


Fig. 11.13 Functional diagram of CSSU (courtesy-Texas Instruments)

T is connected to the ALU input (as a dual 16-bit operand) and is used as local storage in order to minimize memory access.

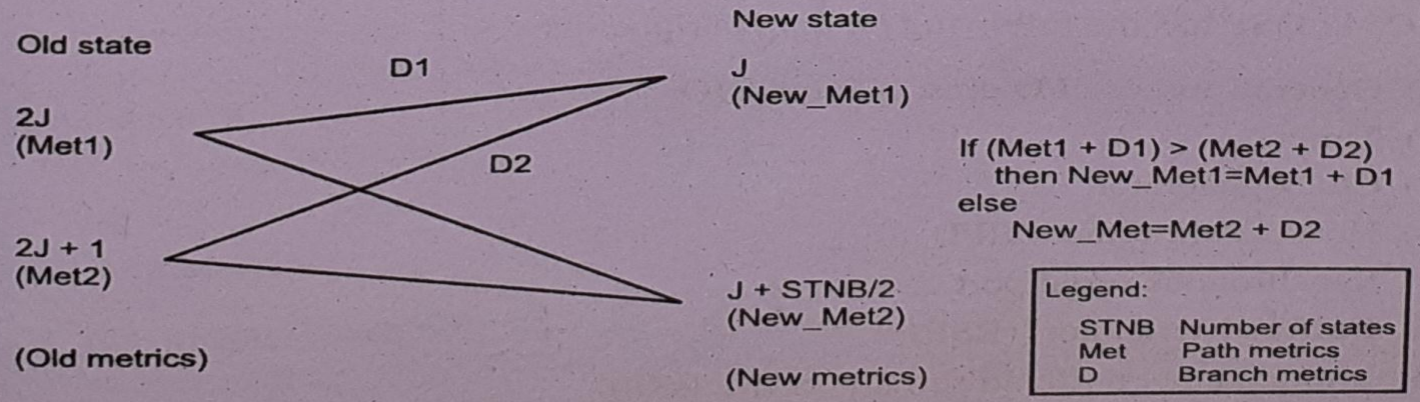


Fig. 11.14 Viterbi Operator (courtesy-Texas Instruments)