FET AMPLIFIER

INTRODUCTION

- Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight.
- JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains.
- The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

INTRODUCTION

- Whereas a BJT device *controls a large output (collector) current by means of a relatively small input (base) current*, the FET device controls an output (drain) current by means ofa small input (gate-voltage) voltage.
- In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device.
- Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs.
- Whereas the BJT has an amplification factor, ß (beta), the FET has a transconductance factor, g_m .

JFET SMALL-SIGNAL MODEL

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \Delta V_{GS}$$

JFET SMALL-SIGNAL MODEL

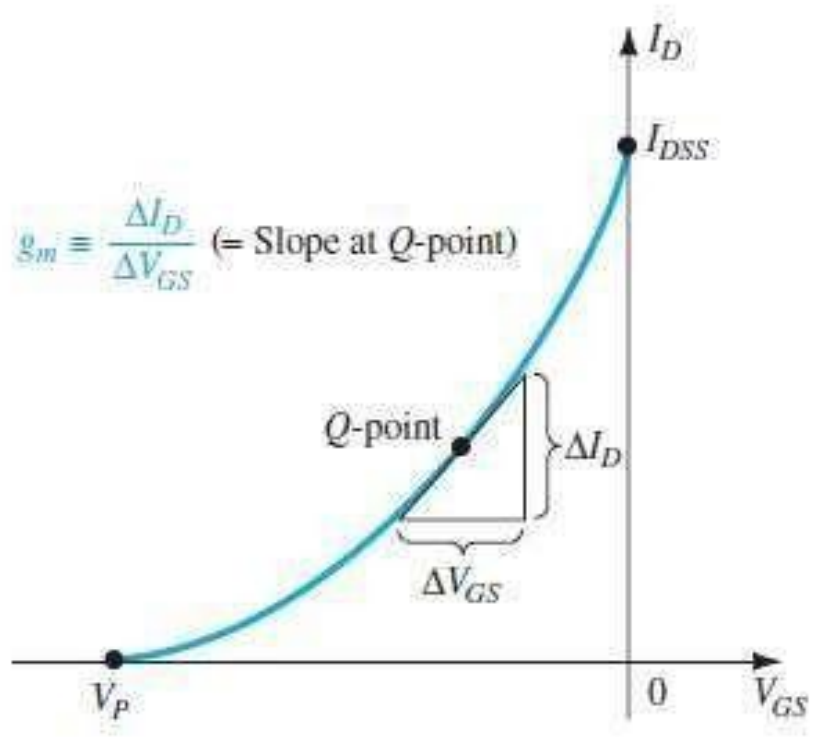
$$\Delta I_D = g_m \Delta V_{GS}$$

- The prefix *trans -* in the terminology applied to g m reveals that it establishes a relationship between an output and an input quantity.
- The root word *conductance* was chosen because *g m* is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor

$$G = 1/R = I/V$$

Solving for *gm*

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



Mathematical Definition of *gm*

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

where 0 *VP* 0 denotes magnitude only, to ensure a positive value for *gm* . It was mentioned earlier that the slope of the transfer curve is a maximum at *VGS* = 0 V.

Plugging in *VGS* = 0 V

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}}$$

where the added subscript 0 reminds us that it is the value of g m when VGS = 0 V

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Equation 1

Example 1:

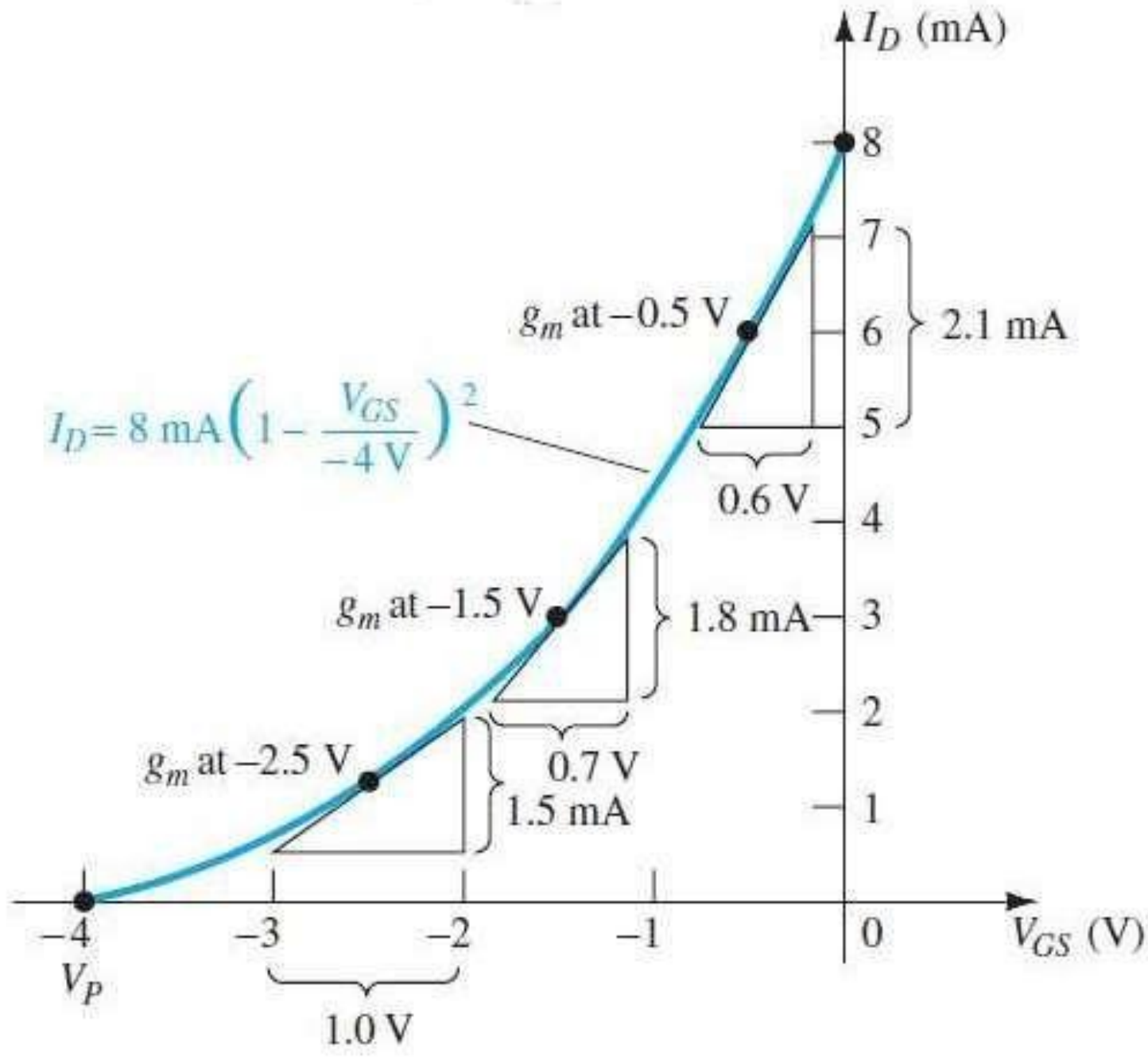
Determine the magnitude of g_m for a JFET with $IDSS$ = 8 mA and VP = -4 V at the following dc bias points:

a. VGS = -0.5 V.

b. VGS = -1.5 V.

c. VGS = -2.5 V.

Solution:


I_D (mA)
8
7
6
5
4
3
2
1
0
V_{GS} (V)
g_m at −0.5 V
$I_D = 8\text{ mA}\left(1 - \frac{V_{GS}}{-4\text{ V}}\right)^2$
2.1 mA
0.6 V
g_m at −1.5 V
1.8 mA
0.7 V
g_m at −2.5 V
1.5 mA
1.0 V
−4
V_P
−3
−2
−1

Solution:

a. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1\ \text{mA}}{0.6\ \text{V}} = \mathbf{3.5\ mS}$$

b. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\ \text{mA}}{0.7\ \text{V}} \cong \mathbf{2.57\ mS}$$

c. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\ \text{mA}}{1.0\ \text{V}} = \mathbf{1.5\ mS}$$

Note the decrease in g_m as V_{GS} approaches V_P

Example 2:

For the JFET having the transfer characteristics of Example 1 :

a. Find the maximum value of g_m .

b.Find the value of g_m at each operating point of Example 1 using Eq. (1) and compare with the graphical results.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$ (vs. 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$ (vs. 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

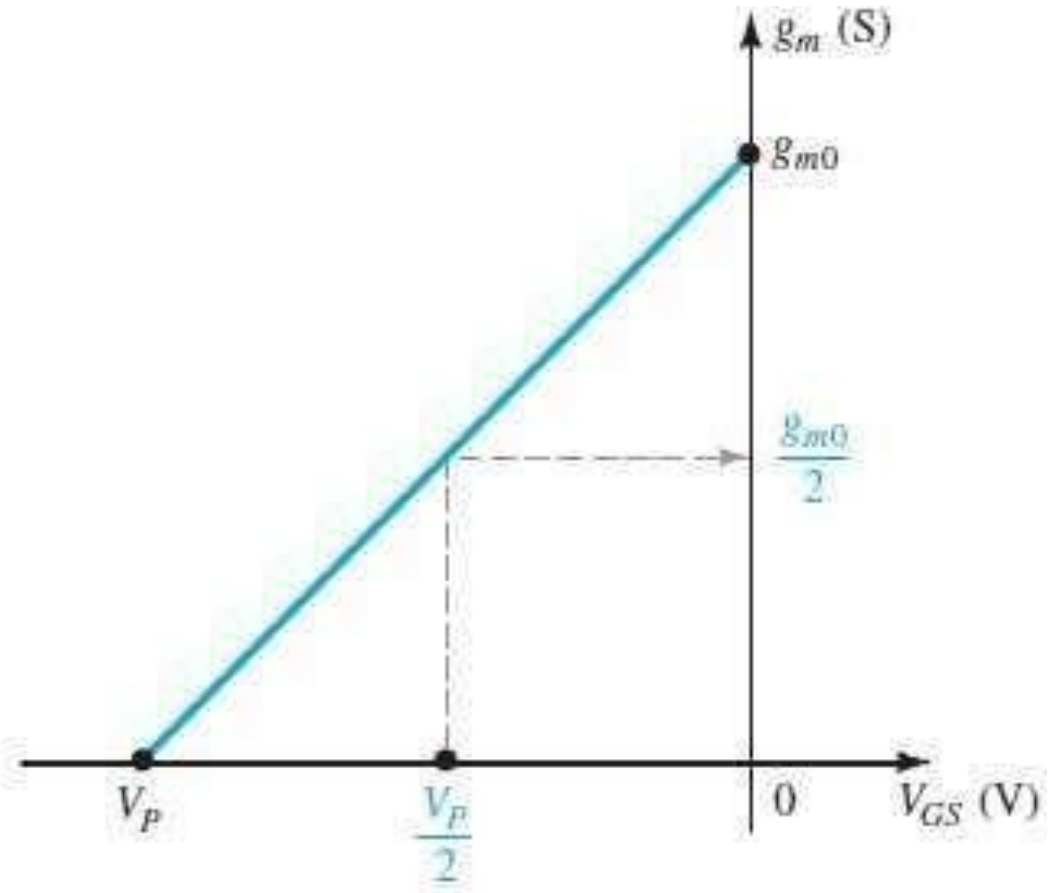
$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$ (vs. 1.5 mS graphically)

On specification sheets, g_m is often provided as g_{fs} or y_{fs}, where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer conductance, and the s indicates that it is connected to the *s*ource terminal.

In equation form,

$$g_m = g_{fs} = y_{fs}$$

In general, therefore ***the maximum value of g m occurs where $V_{GS} = 0V$ and the minimum value at $V_{GS} = V_P$. The more negative the value of VGS the less the value of g_m .***



Plot of g_m versus V_{GS}.

Effect of I_D on g_m

- A mathematical relationship between *g m* and the dc bias current *I D* can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

determine g_m for a few specific values of I_D,

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = g_{m0}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}$$

the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

JFET Input Impedance *Zi*

$$Z_i\,(\text{JFET}) = \infty\,\Omega$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

JFET Output Impedance *Zo*

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

The output impedance of JFETs is similar in magnitude to that of conventional BJTs

the output impedance will typically appear as g_{os} or y_{os} with the units of µS

The parameter y_{os} is a component of an *admittance equivalent circuit* , with the subscript *o* signifying an output network parameter and *s* the terminal (source) to which it is attached in the model.

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

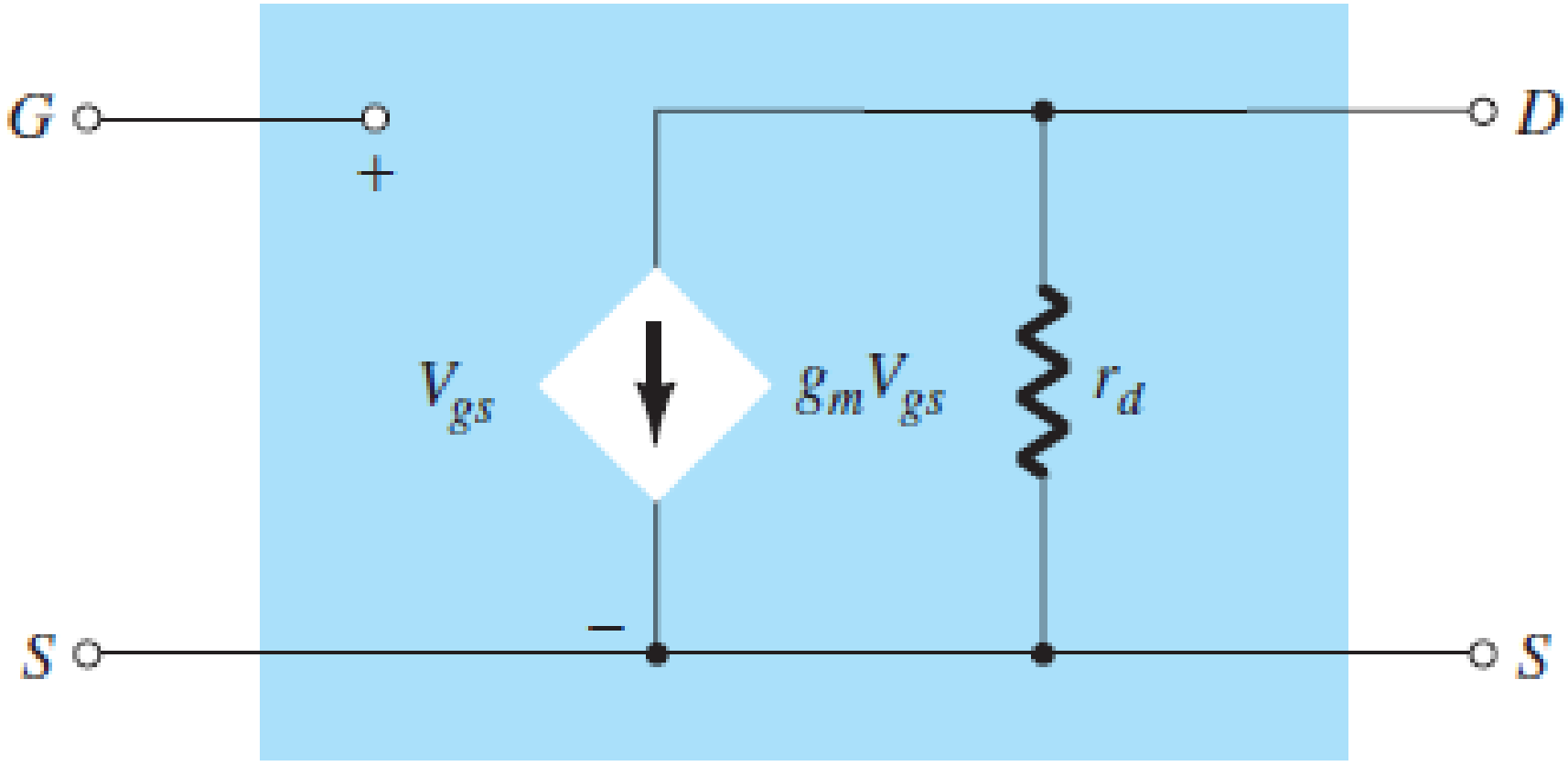
The output impedance is defined on the characteristics as the *slope of the horizontal characteristic curve at the point of operation*.

The *more horizontal the curve*, the *greater is the output impedance*.

If it is *perfectly horizontal*, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

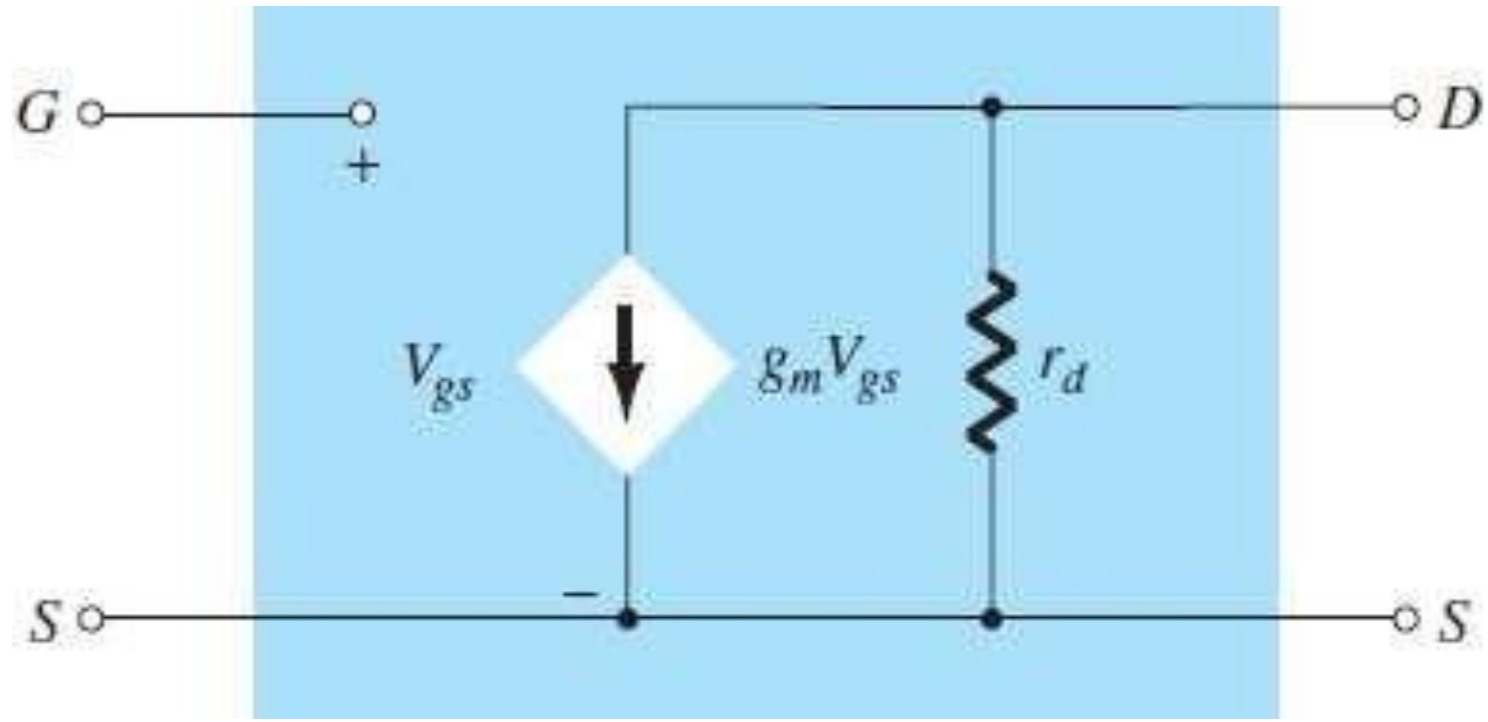
JFET AC Equivalent Circuit



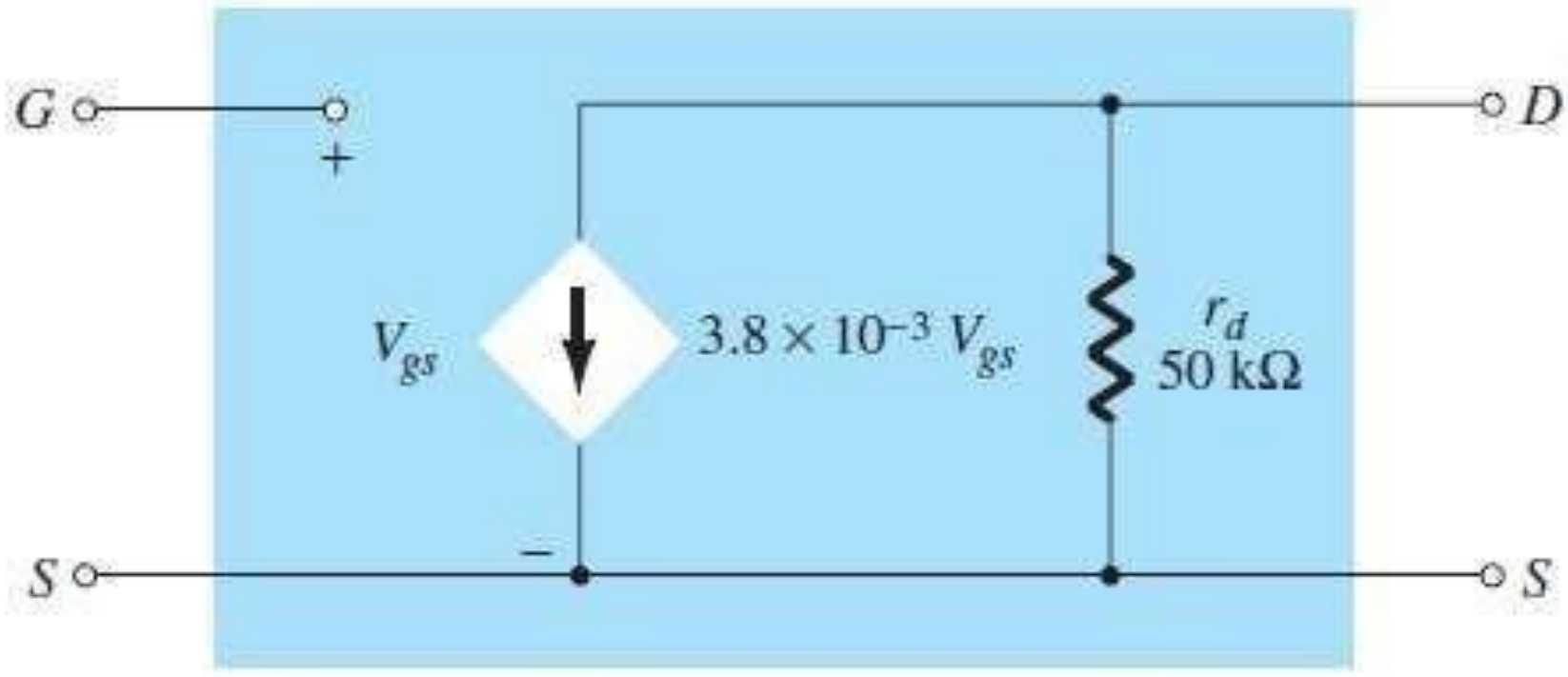
Example 3:

Given $g_{fs} = 3.8\,\text{mS}$ and $g_{os} = 20\,\mu\text{S}$, sketch the FET ac equivalent model.

Soln: (calculate the value of the certain parameters)

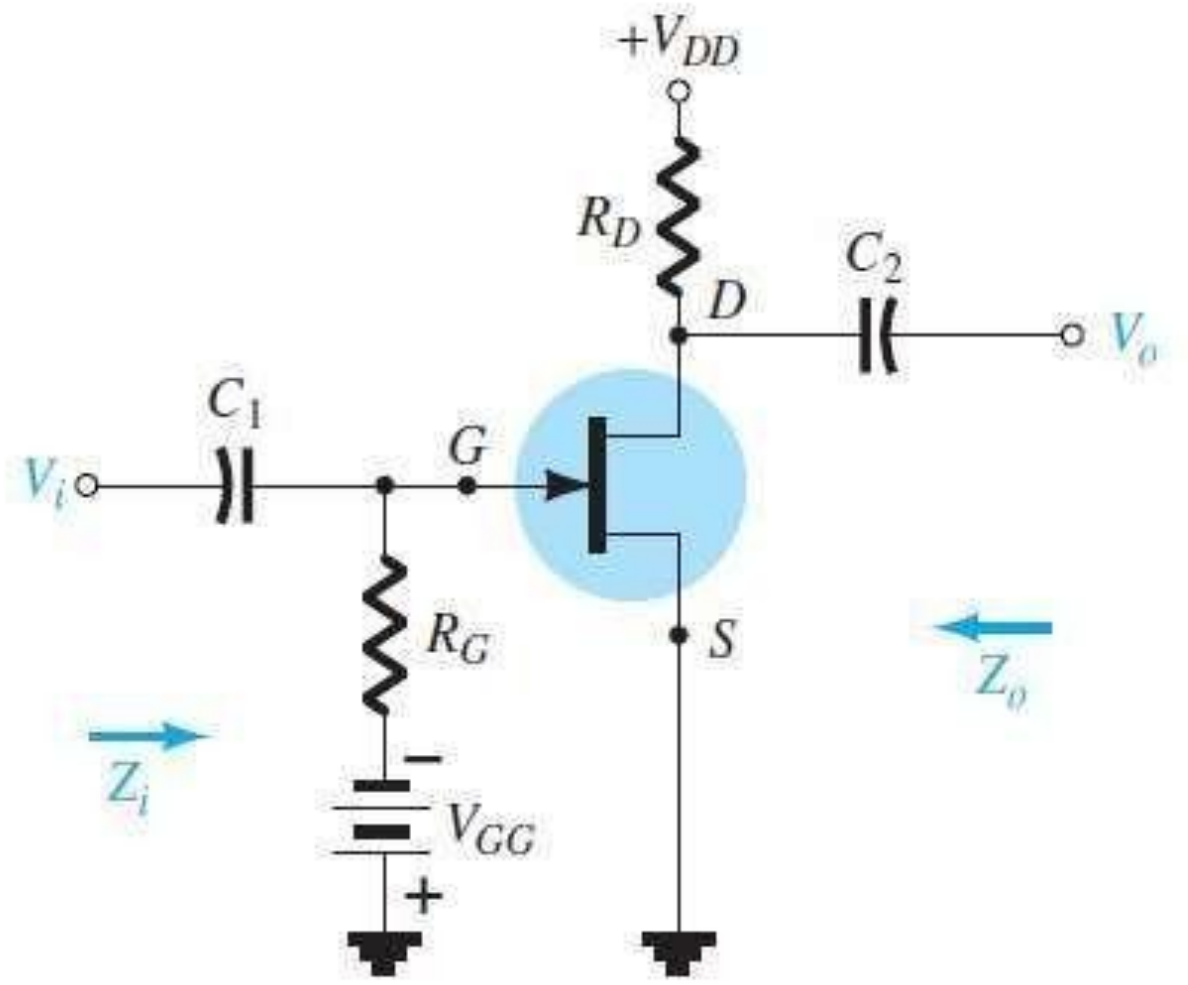


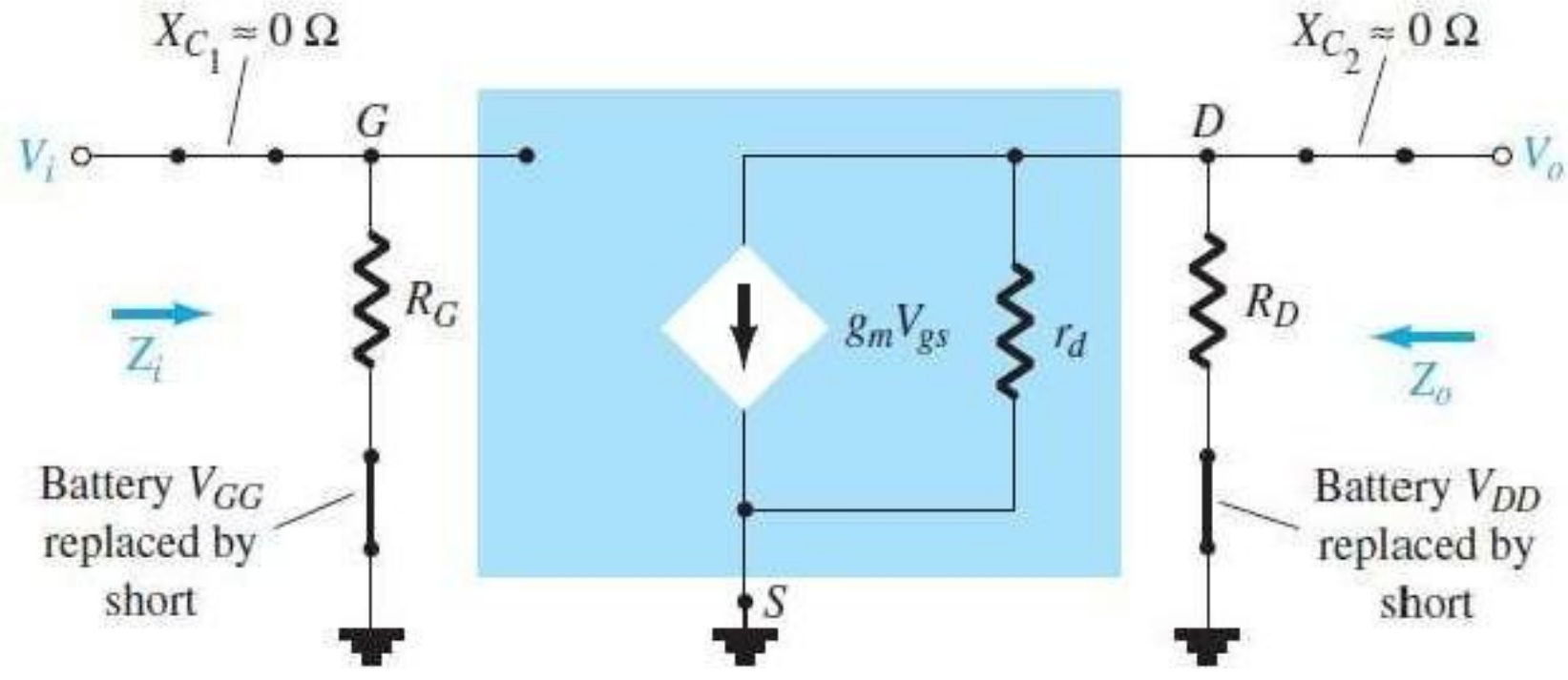
$$g_m = g_{fs} = 3.8\ \text{mS} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

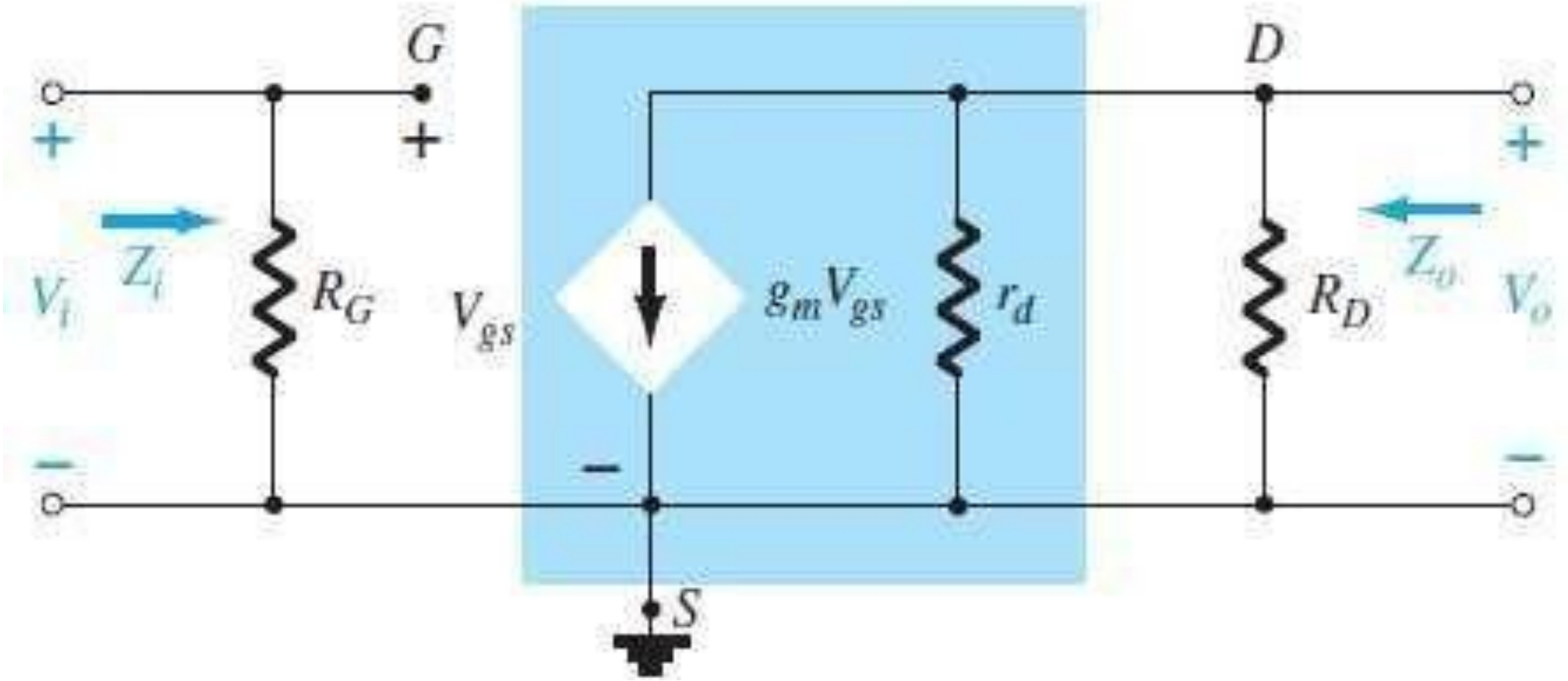


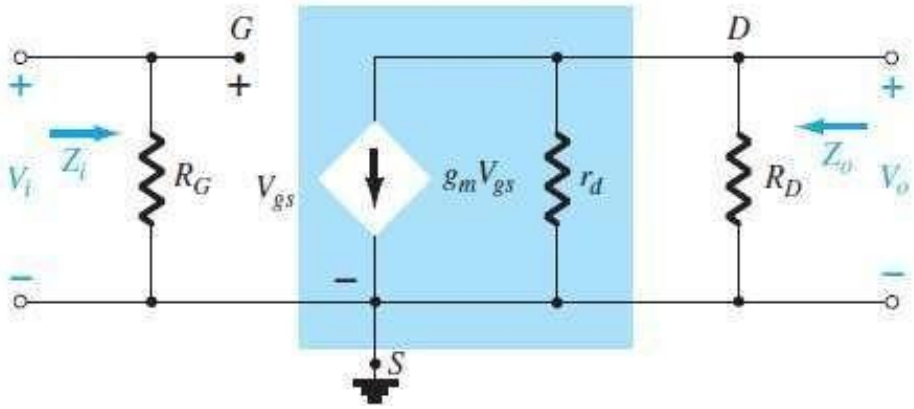
FET CONFIGURATION:

FIXED-BIAS CONFIGURATION




$X_{C_1} \approx 0\ \Omega$
$X_{C_2} \approx 0\ \Omega$
G
D
V_i
V_o
R_G
R_D
$g_m V_{gs}$
r_d
Z_i
Z_o
Battery V_{GG} replaced by short
Battery V_{DD} replaced by short
S


G
D
+
+
+
V_i
Z_i
R_G
V_{gs}
$g_m V_{gs}$
r_d
R_D
Z_o
V_o
−
−
−
S



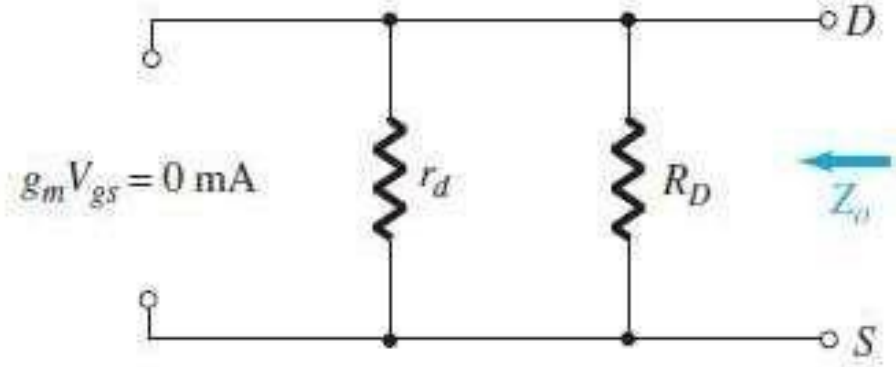
Zi

$$Z_i = R_G$$

because of the infinite input impedance at the input terminals of the JFET.

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$Z_o = R_D \| r_d$$



If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D} \quad r_d \geq 10R_D$$

A_v Solving for V_o, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} = -g_m R_D$$

$r_d \geq 10R_D$

Thank You!

UNIT-III

Small signal analysis of JFET & MOSFET

BJT	FET
1.BJT controls large output(I_c) by means of a relatively small base current. It is a current controlled device.	1.FET controls drain current by means of small gate voltage. It is a voltage controlled device
2.Has amplification factor β	2.Has trans-conductance g_m.
3.Has high voltage gain	3.Does not have as high as BJT
4.Less input impedance	4.Very high input impedance

FET Small-Signal Analysis

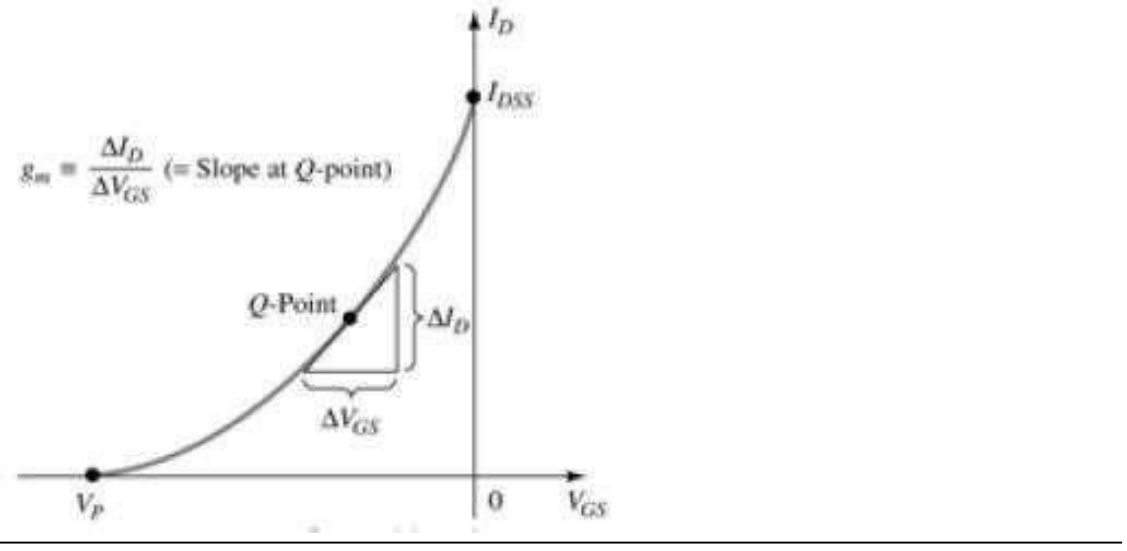
- FET Small-Signal Model
- Trans-conductance

  The relationship of VGS (input) to ID(output)is called trans-conductance.

- The trans-conductance is denoted **gm**.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Definition of g_m using transfer characteristics



Example:

Determine the magnitude of $g_m$for a JFET with I_{DSS} = 8mA and V_P = -4V at the following dc bias points.

a. At V_{GS} = -0.5V

b. At V_{GS} = -1.5V

c. At V_{GS} = -2.5V

Mathematical Definition of gm

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{GS}} \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_p|}\left[1 - \frac{V_{GS}}{V_p}\right]}$$

$$g_m \text{ for } V_{GS} = 0V: \qquad g_{m0} = \frac{2I_{DSS}}{|V_p|}$$

$$\text{for} \quad 1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}} \qquad \boxed{g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}}$$

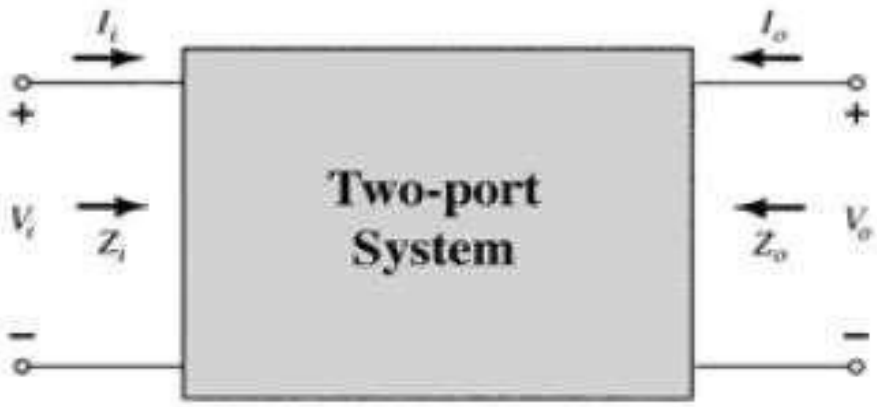
FET Impedance

- Input Impedance Zi : ∞ ohms
- Output Impedance Zo: r_d= 1/yos

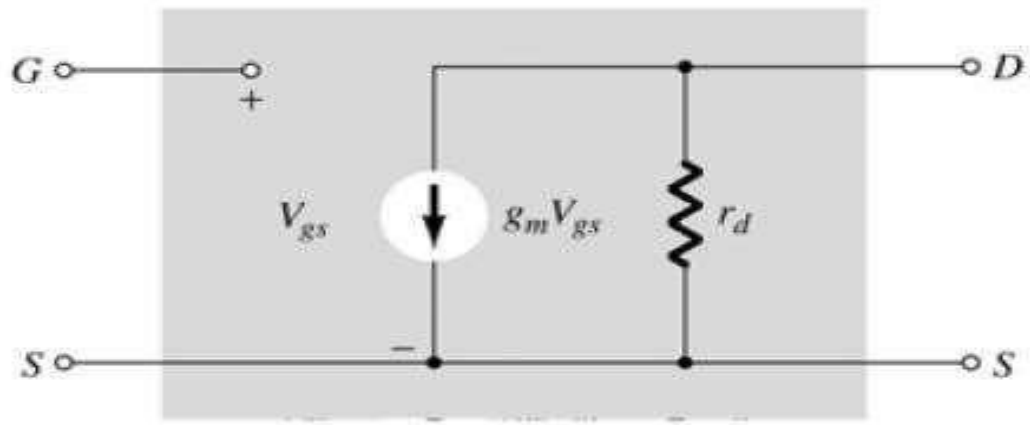
$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}\ =\ \text{constant}}$$

Yos=admittance equivalent circuit parameter listed on FET specification sheets.

Two port model



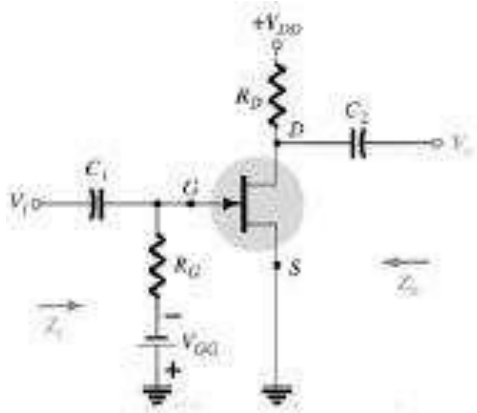
FET AC Equivalent Circuit



Phase Relationship

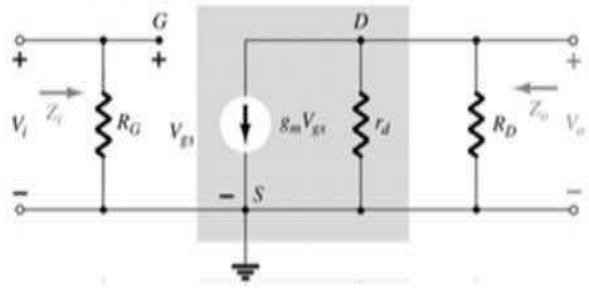
- The phase relationship between input and output depends on the amplifier configuration circuit.
- Common – Source ~ 180 degrees
- Common - Gate ~ 0 degrees
- Common – Drain ~ 0 degrees

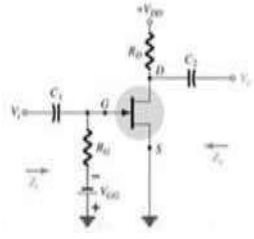
JFET Common-Source (CS) Fixed-Bias Configuration



- The input is on the gate and the output is on the drain.
- Fixed bias configuration includes the coupling capacitors c1 and c2 that isolate the dc biasing arrangements from the applied signal and load.
- They act as short circuit equivalents for the ac analysis.

AC Equivalent Circuit



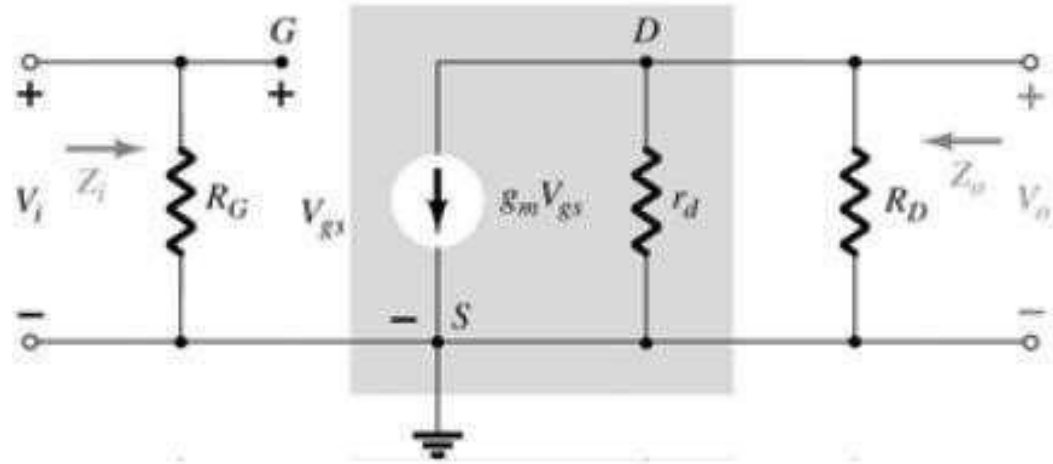


Input impedance $Zi=R_G$

Output Impedance: $Z_O = r_d \ \ R_D$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain



$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10R_D}$$

$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

Phase difference

Negative sign in the gain expression indicates that the output voltage is 180^0 phase shifted to that of input.

Example

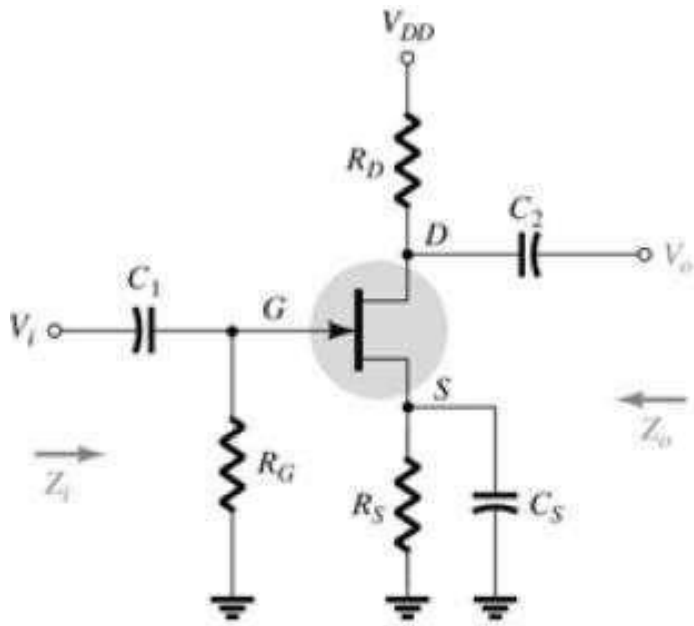
For fixed bias circuit, the following bias data are given. V_{GS}=-2V, I_{DO}=5.625mA and V_p=-8V. The input voltage v_i. The value of y_{Os}=40μS.

1. Determine G_m
2. Find r_d
3. Determine Z_i
4. Calculate Z_O, A_V with and without effects of r_d.

JFET Self bias configuration

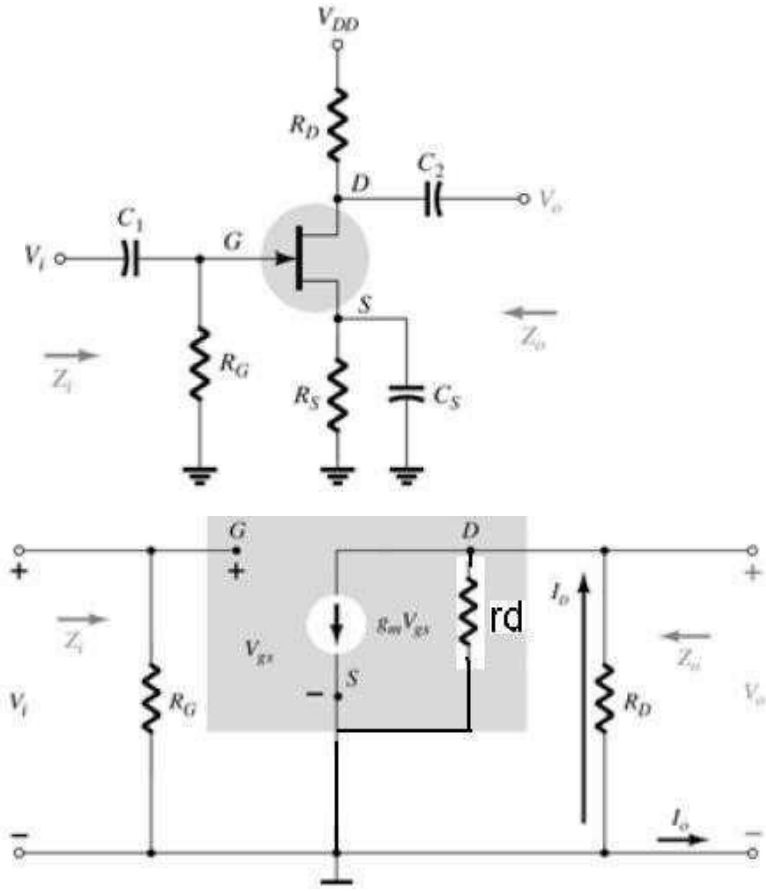
- Main disadvantage of fixed bias configuration requires two dc voltage sources.
- Self bias circuit requires only one DC supply to establish the desired operating point.

Self bias configuration



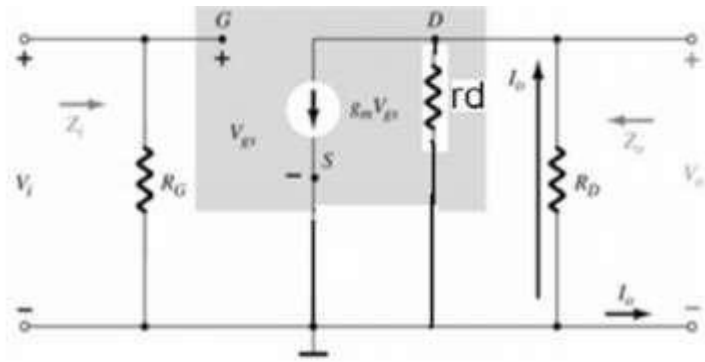
If Cs is removed, it affects the gain of the circuit

AC Equivalent Circuit



- The capacitor across the source resistance assumes its short circuit equivalent for dc allowing R_S to define the operating point.
- Under ac conditions the capacitors assumes short circuit state and short circuits the R_s.
- If R_S is left un-shorted, then ac gain will be reduced.

Redrawn equivalent circuit:



Here R_s is bypassed by X_{Cs}

Circuit parameters:

- Since the resulting circuit is same as that of fixed bias configuration, all the parameter expression remains same as evaluated for fixed bias configuration.
- Input impedance $Zi=R_G$
- Output Impedance:$Z_O=$ r_d parallel R_D

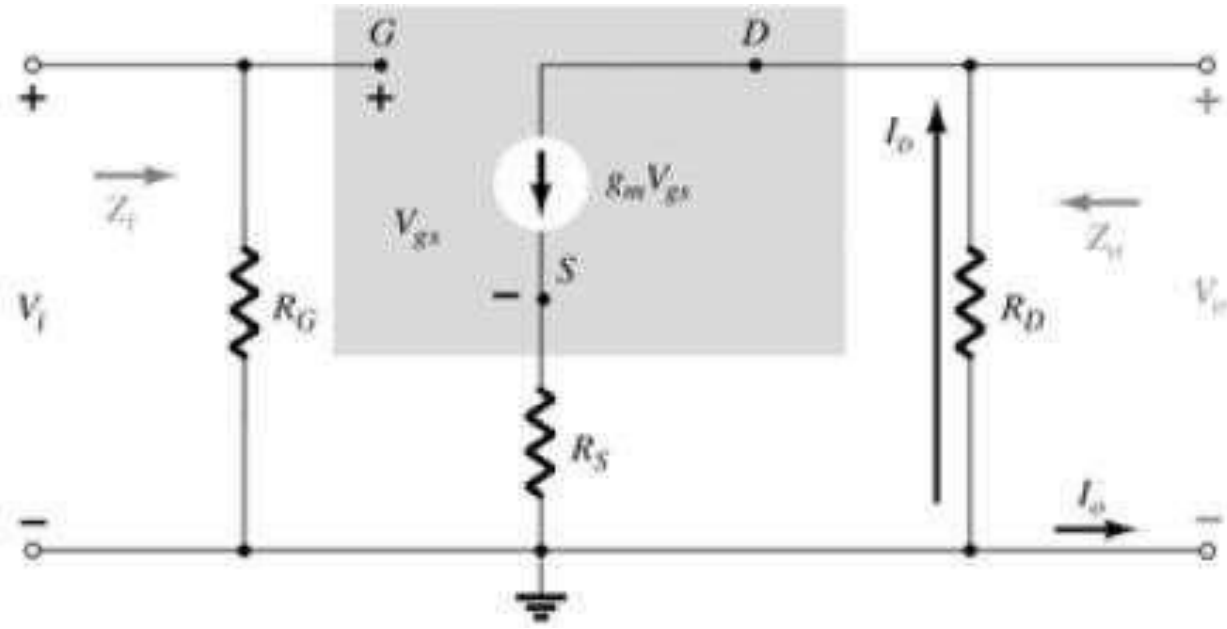
$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Leaving Rs un-bypassed helps to reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

$$A_v = -g_m(r_d \,||\, R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Self bias configuration with un bypassed R_s



- Here R_s is part of the equivalent circuit .
- There is no way to reduce the network with lowest complexity.
- Carefully all the parameters have to be calculated by considering all polarities properly

Input Impedance

- Due to open-circuit condition between gate and output network, the input impedance remains as follows:

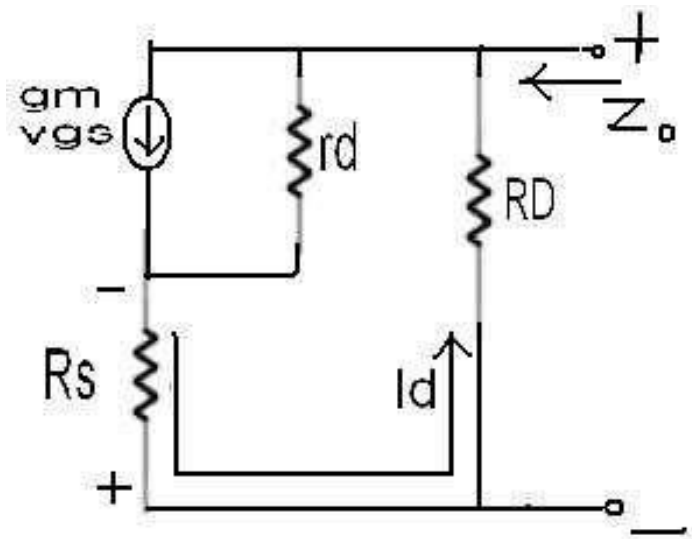
$$Z_i = R_G$$

Output impedance

- Output impedance is defined by

  ZO= Vo/Io at vi=0

Setting Vi=0 results in following circuit.



$$Zo = \frac{RD}{1 + gmRs + \frac{RD + Rs}{rd}}$$

$$rd > 10(RD + Rs)$$

$$Zo = \frac{RD}{1 + gmRs}$$

Voltage gain:

$$Av = \frac{Vo}{Vi} = \frac{gmRD}{1 + gmRs + \frac{RD + Rs}{rd}}$$

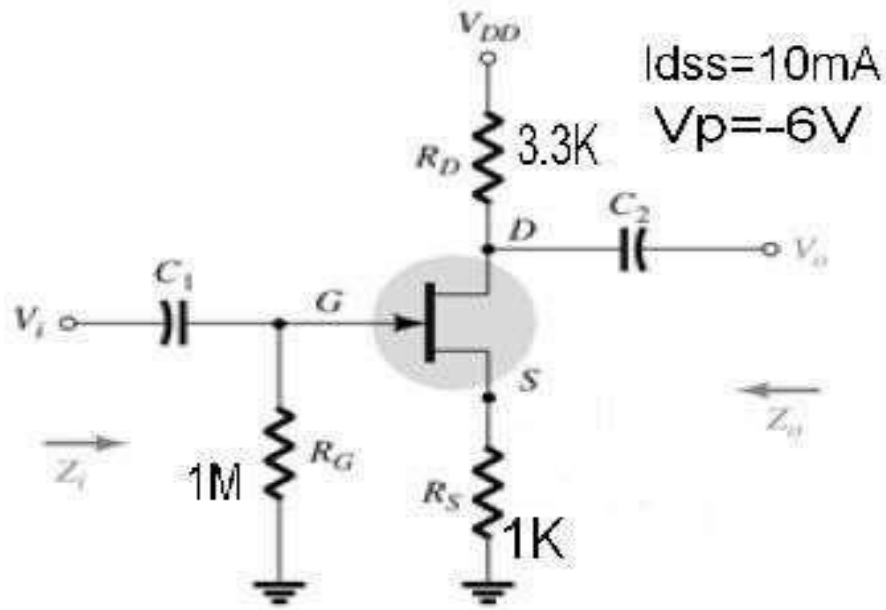
$$rd \geq 10(RD + Rs), Av = -\frac{gmRD}{1 + gmRs}$$

Example: A self bias circuit has operating point defined by VGSo=-2.6V, IDq=2.6mA with IDSS=8mA and Vp=-6V.

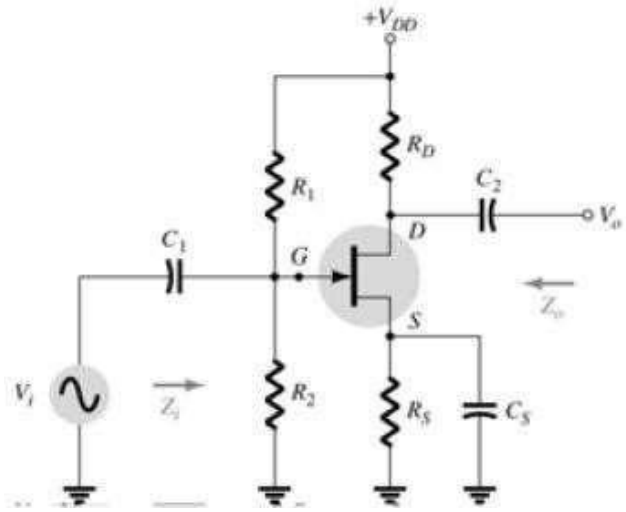
Yos=20uS

Determine

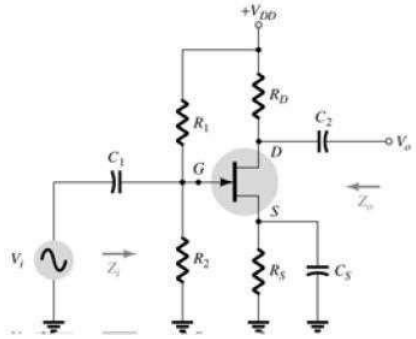
a. **Gm**
b. **Rd**
c. **Zi**
d. **Zo with and without rd effect.**
e. **Av with and without rd effect**



JFET voltage divider configuration



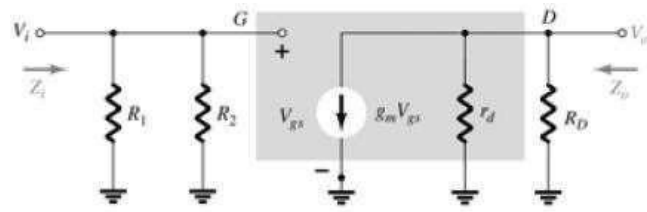
AC equivalent circuit



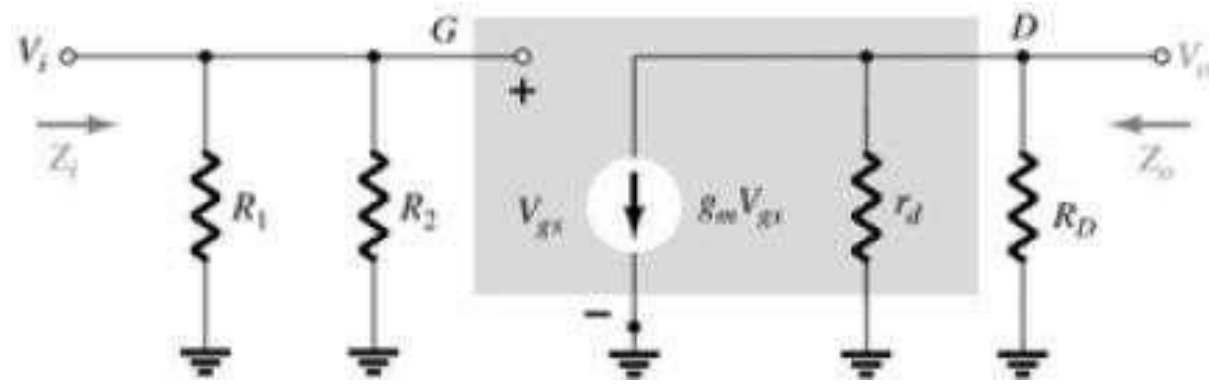
Input Impedance: $Z_i = R_1 \| R_2$

Output Impedance: $Z_o = r_d \| R_D$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:



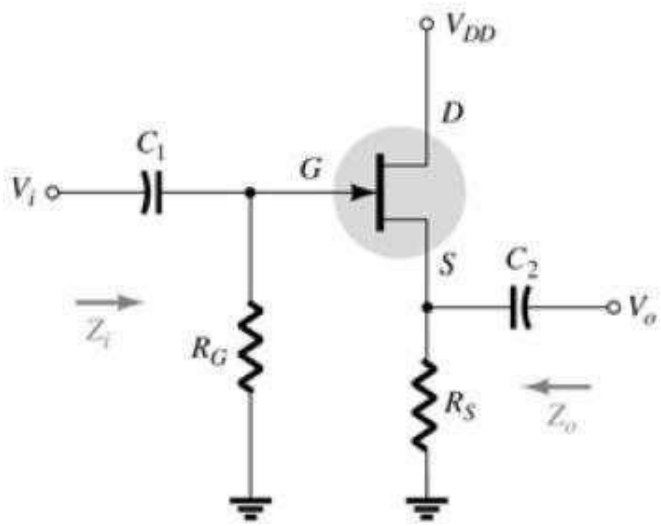
$$A_v = -g_m(r_d \,||\, R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Note

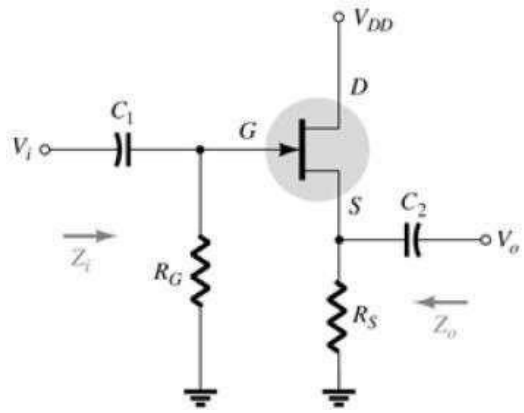
- Equations for ZO and Av are same as in fixed bias.
- Only Zi is now dependent on parallel combination of R1 and R2.

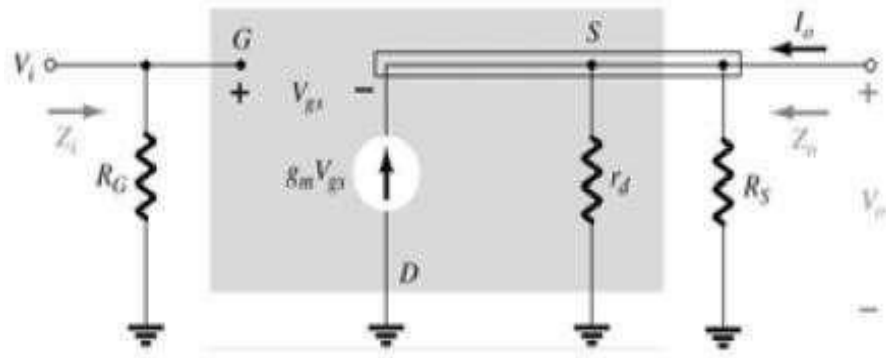
JFET source follower



In a CD amplifier configuration the input is on the gate, but the output is from the source.

AC equivalent circuit





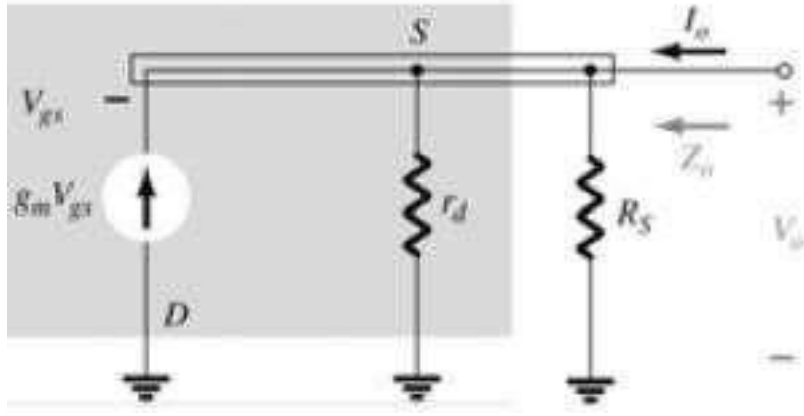
Input and output impedance:

- **Input impedance** : Zi=RG

- **Output impedance** :

setting Vi=0V will result in the gate terminal being connected directly to ground as shown in figure below.

Equivalent circuit



- **Applying KCL at output node**

$$I_o + g_m V_{gs} = I_{rd} + I_{RS}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_s}$$

$$result : I_o = V_o \left[\frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs}$$

$$= V_o \left[\frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs}$$

$$= V_o \left[\frac{1}{r_d} + \frac{1}{R_s} \right] - g_m [-V_o]$$

$$= V_o \left[\frac{1}{r_d} + \frac{1}{R_s} + gm \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{\left[\frac{1}{r_d} + \frac{1}{R_s} + g_m\right]} \frac{1}{V_0}$$

$$= \frac{1}{\left[\frac{1}{r_d} + \frac{1}{R_s} + g_m\right]}$$

$$Z_o \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10R_S}$$

rd, Rs and gm are all in parallel.

Voltage gain

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$$

$$A_v = \frac{g_m R_S}{1 + g_m R_S} \Big|_{r_d \geq 10R_S}$$

Since denominator is larger by a factor of one, the gain can never be equal to or greater than one. (as in the case of emitter follower of BJT)

Example:

A dc analysis of the source follower has resulted in VGS=-2.86V and Io=4.56mA.

Determine

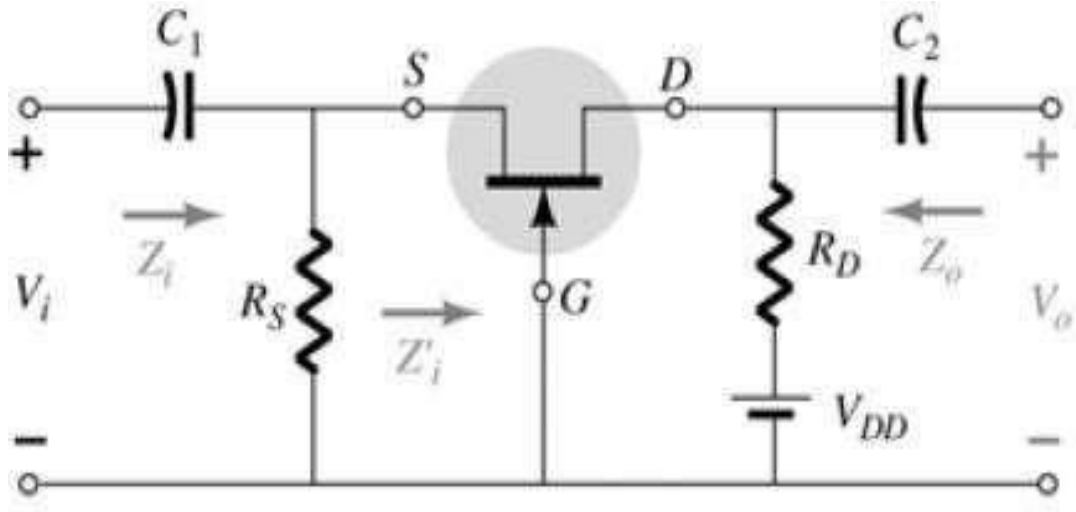
a. **gm**
b. **Zi**
c. **rd**
d. **Calculate Zo with and without effect of rd.**
e. **Calculate Av with and without effect of rd.**

Compare the results.

Given IDSS=16mA, Vp=-4V, yos=25µS.

The coupling capacitors used are 0.05µF.

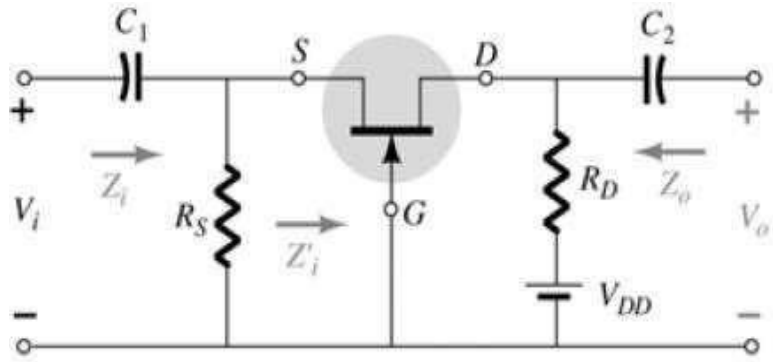
JFET common gate configuration

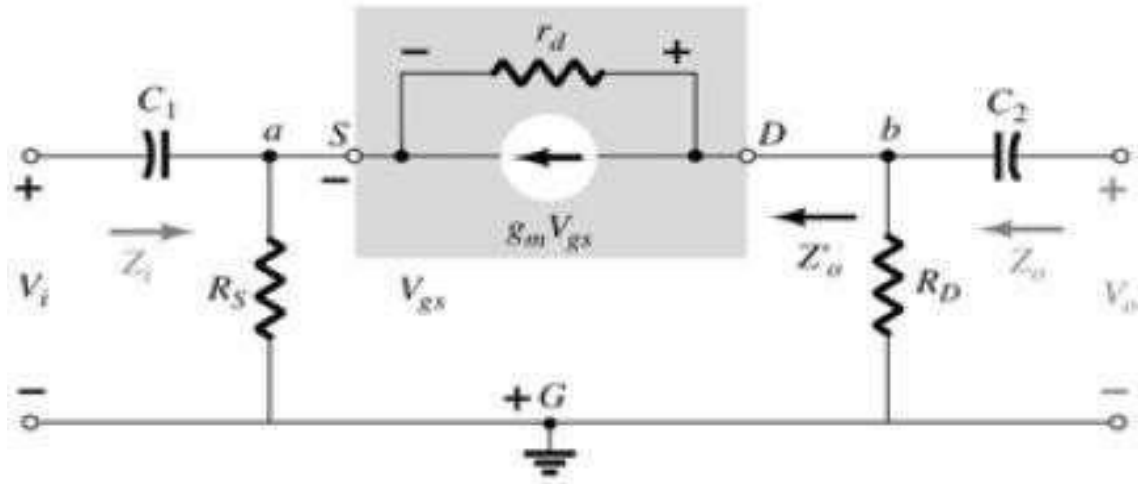


The input is on source and the output is on the drain.

Same as the common base in BJT

AC equivalent circuit





Impedances:

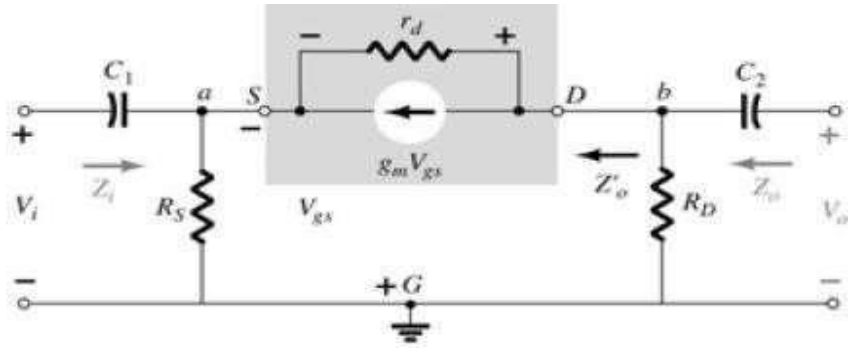
Input Impedance: $Z_i = R_S \| \left[\dfrac{r_d + R_D}{1 + g_m r_d} \right]$

$$Z_i \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10R_D}$$

Output Impedance: $Z_o = R_D \| r_d$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain



$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]}$$

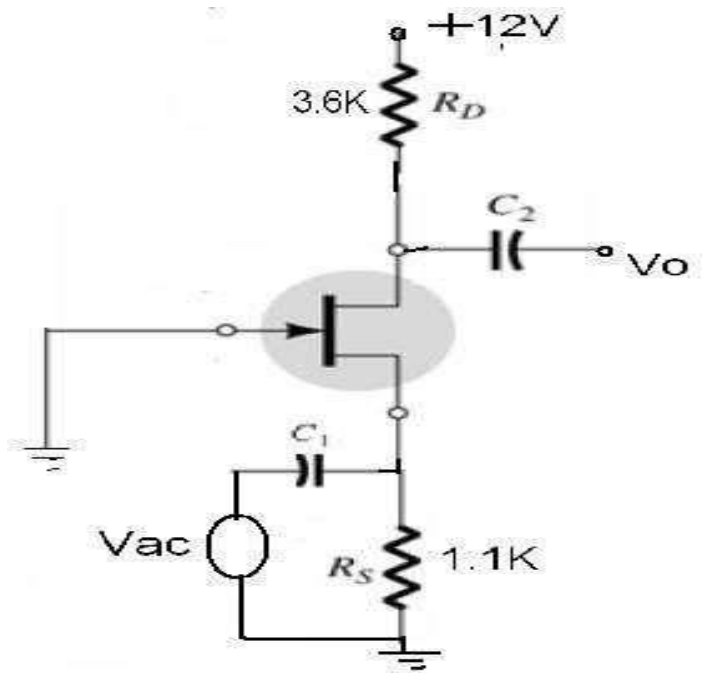
$$A_v = g_m R_D \Big|_{r_d \geq 10 R_D}$$

Example: For the network shown if VGSo=-2.2V, IDoq=2.03mA,

Determine gm,rd, Zi with and without the effect of rd, Av with and without the effect of rd.

Also find Vo with and without rd. compare the results.

C1 and c2 are given by 10uf.

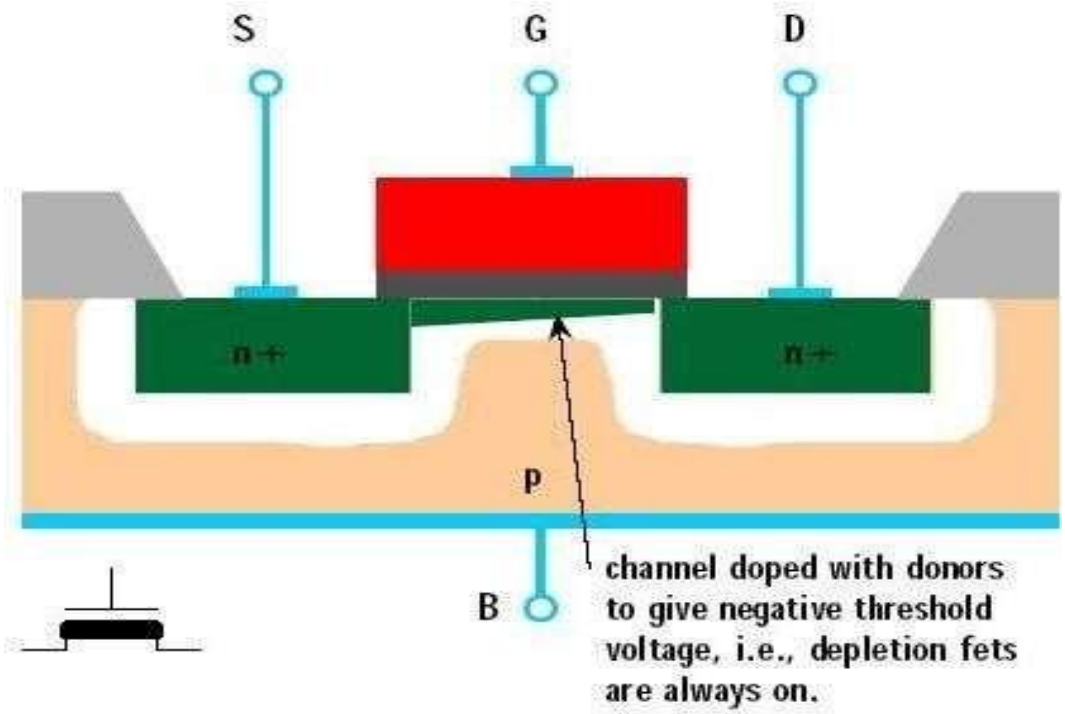


MOSFETs:

MOSFETs are of two types;

- Depletion type
- Enhancement type

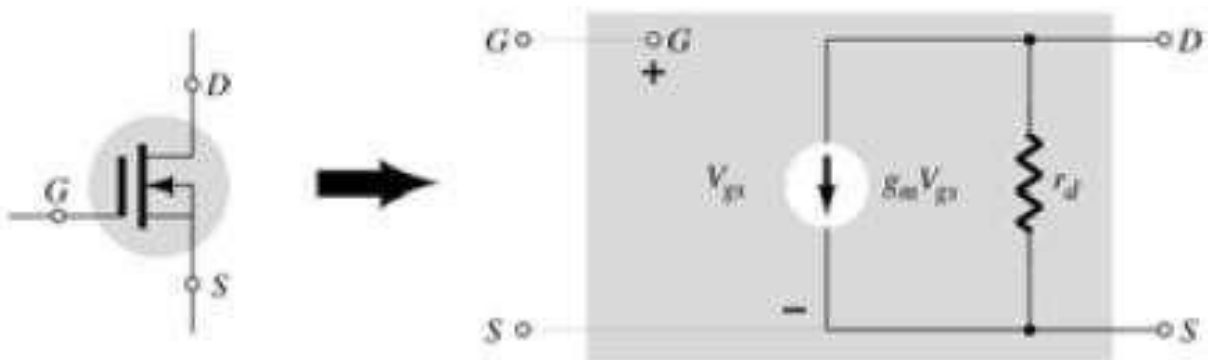
1. Depletion type MOSFETs



- Shockley's equation is also applicable to depletion type MOSFETs.
- This results in same equation for gm.
- The ac equivalent model for this MOS device is same as JFET.
- Only difference is V**GSo** is positive for n-channel device and negative for p-channel device.
- As a result of this, gm can be greater than gmo.

- Range of rd is very similar to that of JFETs.

D-MOSFET ac equivalent model



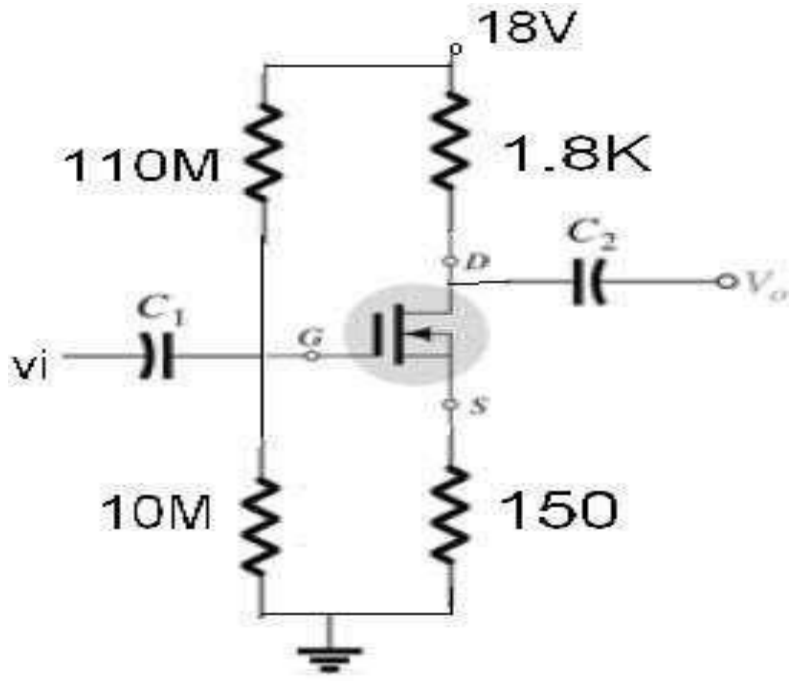
Example:A network shown below has the dc analysis results as
IDSS=6mA, VP=3V,VGSo=1.5V and IDQ=7.6mA.yos=10uS

a. Determine gm and compare with gmo

b. Find rd

c. Sketch ac equivalent circuit

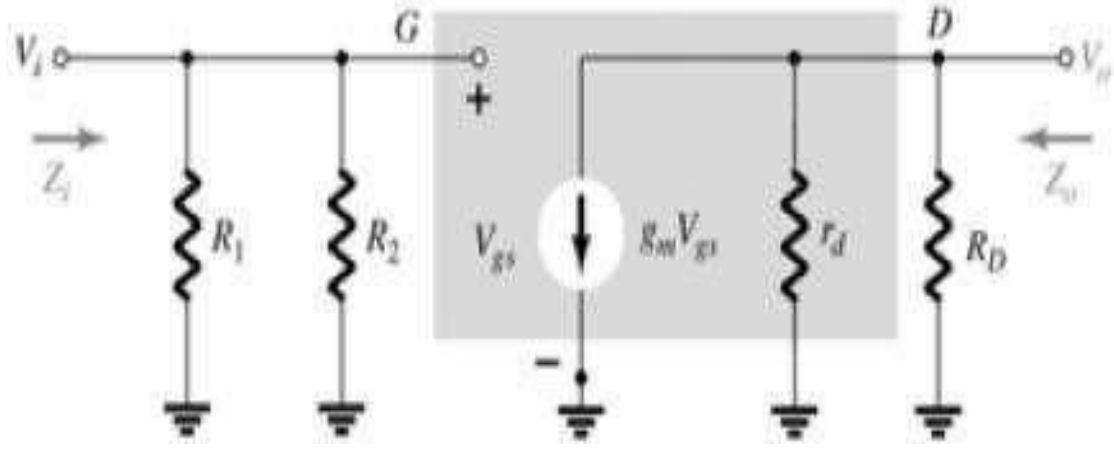
d. Find Zi,Zo and Av.



Solution:

- gmo=4mS
    - gm=6mS
    - gm is 50% more than gmo
    - rd= 100K Ω
    - Zi=10M Ω parallel with 110M Ω =9.17MΩ
    - Zo=100K Ω parallel with 1.8K Ω=1.8KΩ
- Av=-gmrd= 10.8

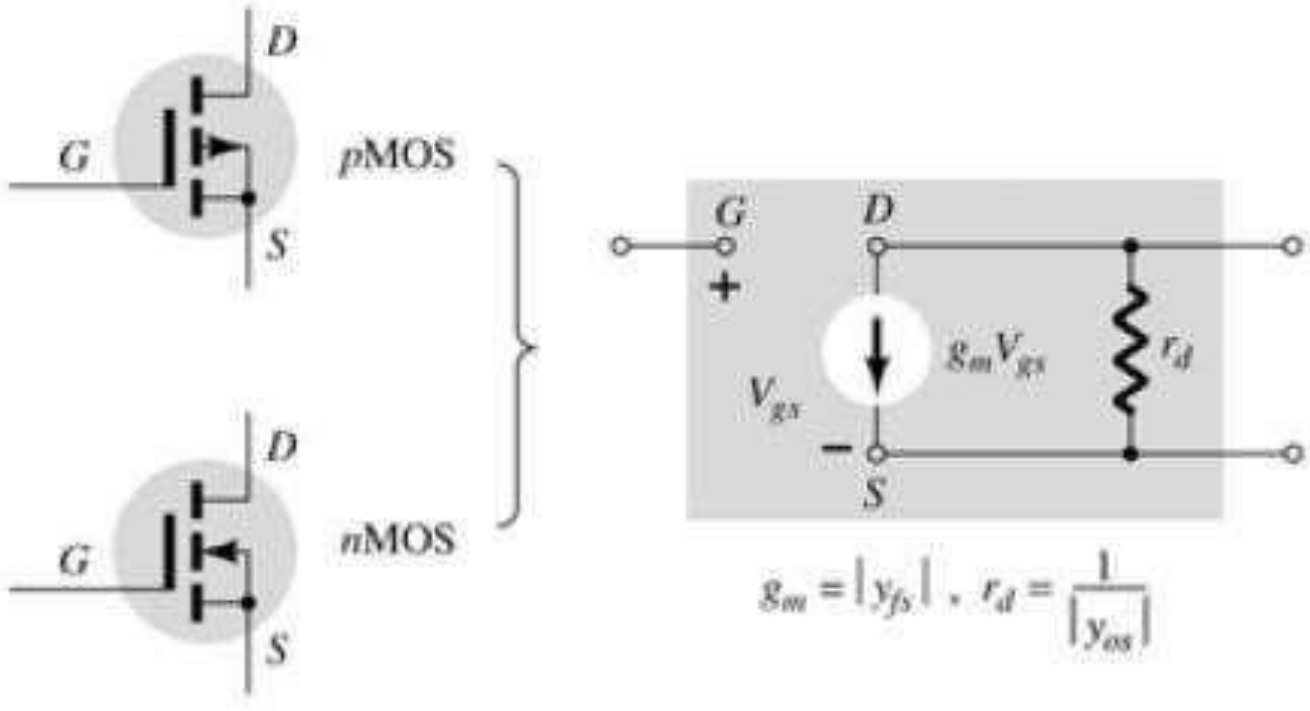
Ac equivalent circuits



Enhancement type MOSFET

- There are two types of E-MOSFETs: nMOS or n-channel MOSFETs pMOS or p-channel MOSFETs

E-MOSFET ac small signal model

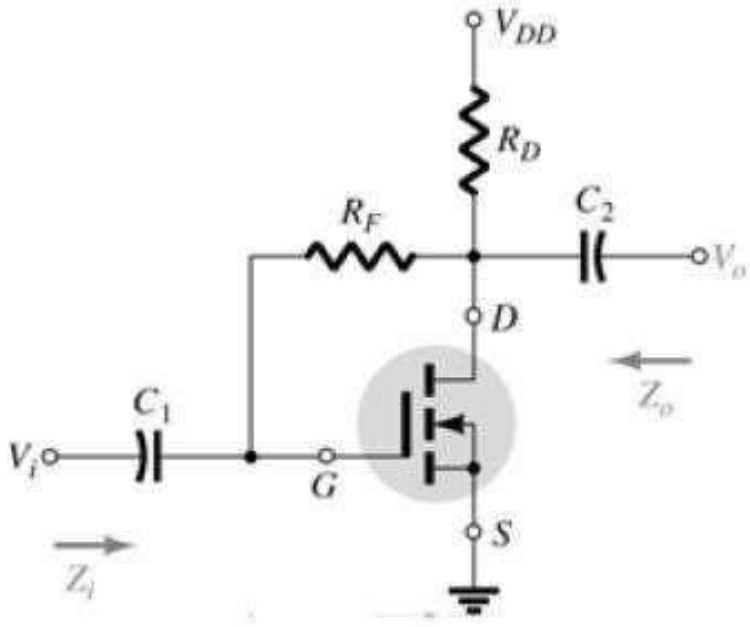


- **ID=k(VGS-VGS(Th))2**
- **gm is defined by**

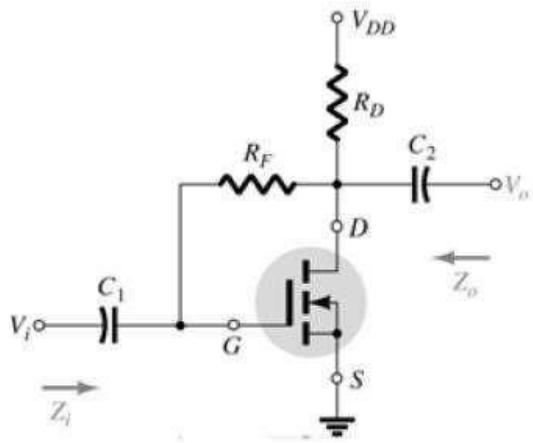
- **Taking the derivative and solving for gm,**

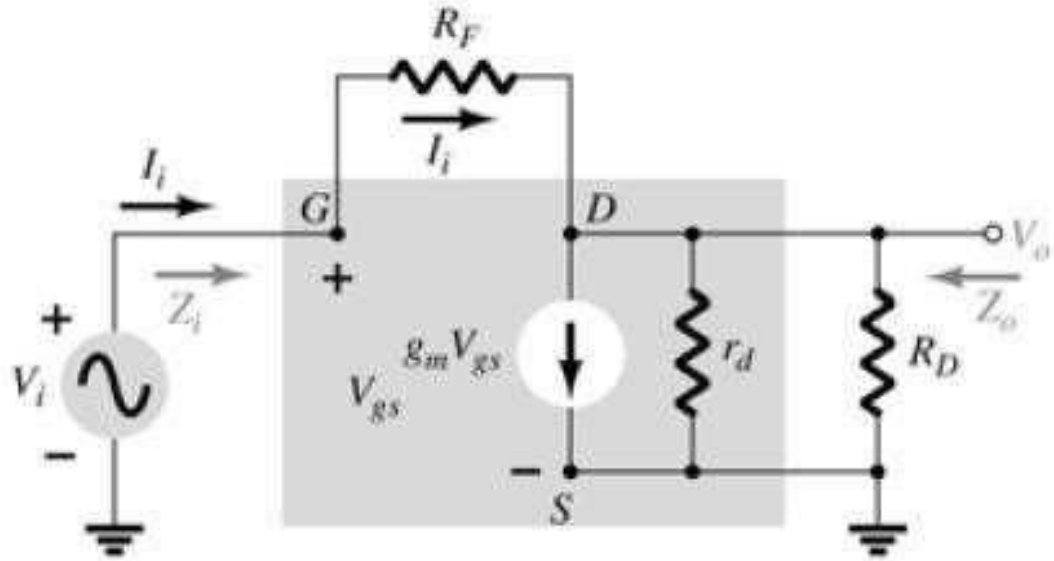
gm=2k(VGS-VGS(th))

EMOSFET drain feedback configuration



Ac equivalent model





Input and output impedances

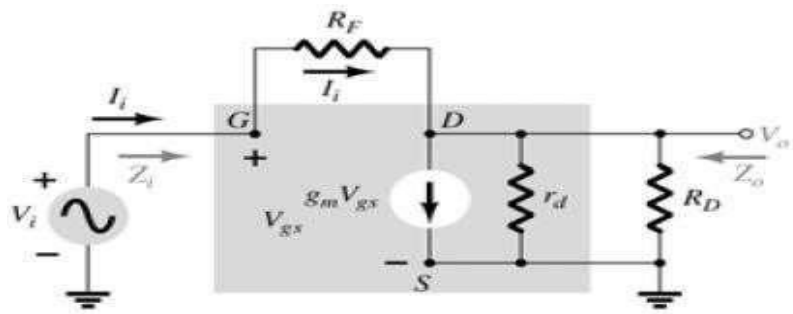
Input Impedance: $Z_i = \dfrac{R_F + r_d \,\|\, R_D}{1 + g_m (r_d \,\|\, R_D)}$

$$Z_i \cong \frac{R_F}{1 + g_m R_D}\Bigg|_{R_F >> r_d \| R_D,\ r_d \geq 10 R_D}$$

Output Impedance: $Z_o = R_F \,\|\, r_d \,\|\, R_D$

$$Z_o \cong R_D \Big|_{R_F >> r_d \| R_D,\ r_d \geq 10 R_D}$$

Voltage gain

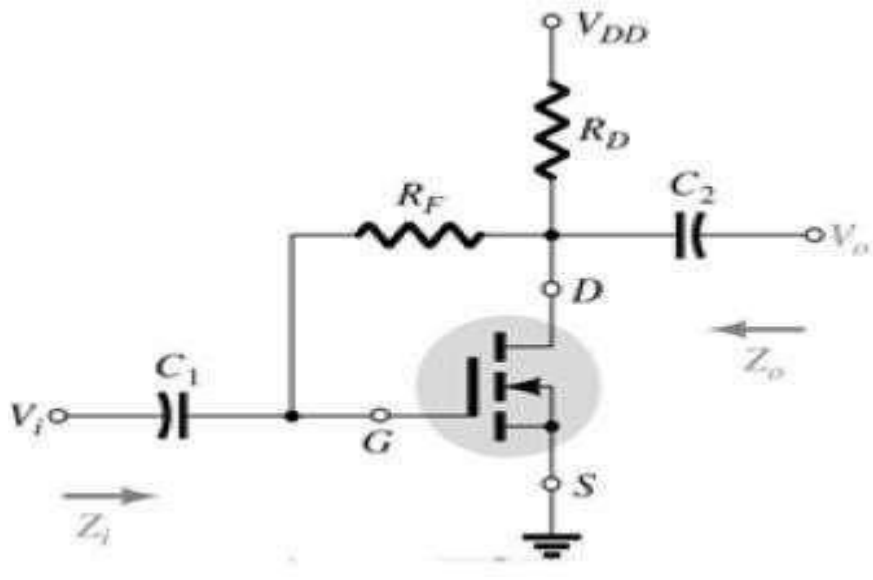


$$A_v = -g_m (R_F \,\|\, r_d \,\|\, R_D)$$

$$A_v \cong -g_m R_D \Big|_{R_F >> r_d \| R_D,\ r_d \geq 10 R_D}$$

Numerical

For the above said configuration, the following results were got. $K=0.24X10^{-3}A/V^2$, $V_{gsQ}=6.4V$, $I_{DQ}=2.75mA$. Determine gm, rd, Z_i with and without the effect of rd, Z_o with and without the effect of rd. Av with and without effect of rd. And compare the results. Id(sat)=6mA, VGS(th)=3V, VGS(on)=6V,yos=20uS.



- **R_D=2K ohms**
- **R_F=10M ohms**
- **C1,c2=1uF**

Solution.

- **gm=2k(V_{GS}-$V_{GS(th)}$)**

  =1.63mS.
- **rd=1/yos=50KΩ**
- **Zi with rd:**

$$Zi = \frac{R_f + (r_d // R_D)}{1 + g_m(r_d // R_D)}$$

= 2.42MΩ

- **Zi without effect of rd:** $Z_i = \frac{R_F}{1 + g_m R_D}$

  = 2.53MΩ

- **Zo with rd: (R_F parallel r_d parallel R_D)**

  = 1.92KΩ

- **Zo without rd: Zo=RD = 2KΩ**

- Gain A_V with r_d:

$$A_v = -g_m\left(R_F \parallel r_d \parallel R_D\right)$$

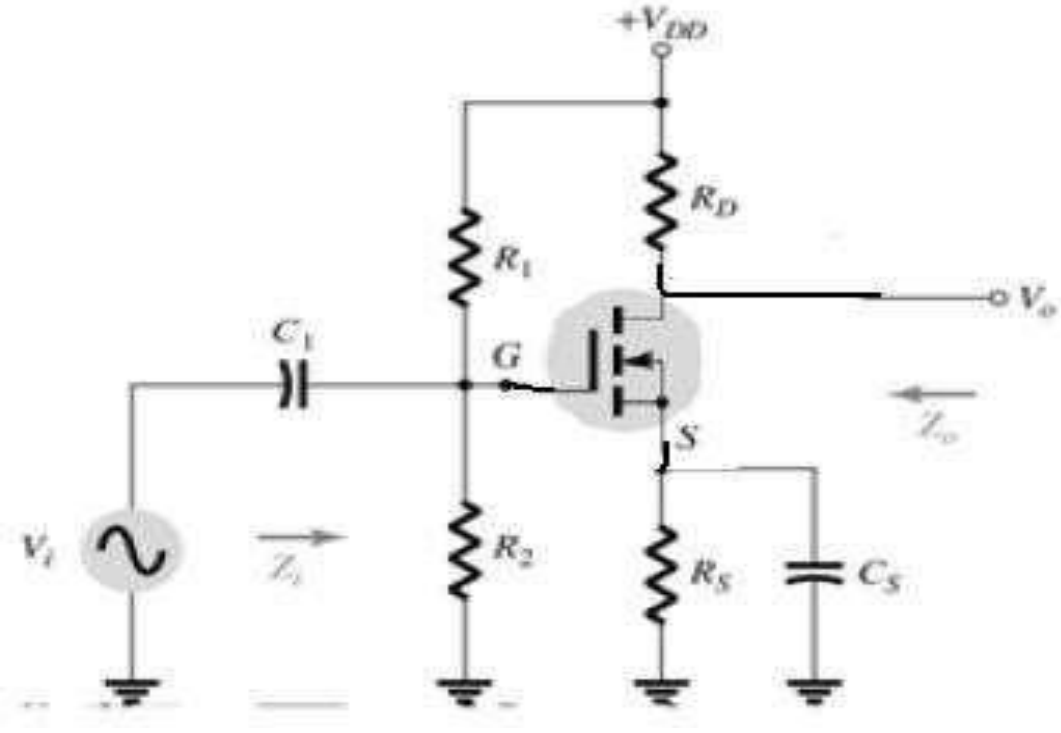
- = -3.21

- Without effect of rd:

$$A_v \cong -g_m R_D$$

- = -3.26

E MOSFET voltage divider configuration



Important Parameters

Input Impedance: $Z_i = R_1 \| R_2$

Output Impedance: $Z_o = r_d \| R_D$

$$Z_o \cong R_D \big|_{r_d \geq 10R_D}$$

$$A_v = -g_m (r_d \| R_D)$$

$$A_v = -g_m R_D \big|_{r_d \geq 10R_D}$$

Ac equivalent circuit